

# Monet 14 " Intel Skylake Platform Block Diagram

Channel A

DDR3L SO-DIMM  
PAGE 17

1600 MT/s 1.35V

**CPU**  
**Skylake - U**

Processor : Dual Core  
Power : 15 (Watt)  
Package : BGA1356  
Size : 42 x 24 \* 1.16 (mm)

GPU

**Nvidia**  
**N16S-GM**

23mm X 23mm (GB2b-64)  
596 ball

PAGE 18~21

Dual Rank

DDR3L (2GB/4GB)

PAGE 22~25

HDD  
PAGE 31

SATA3 6GB /S Port 7

DMIC\*2

DB

HP+MIC Jack

DB

SPEAKER

DB

Audio Codec  
Conexant  
**CX6008**  
2 Watt

HDA

I2C

SPI

Flash ROM  
4 MB  
PAGE 34

Flash ROM  
8 MB  
PAGE 34

Touch Pad  
PAGE 32

K/B  
PAGE 33

FAN  
PAGE 37

SPI

PS/2

HSPI

LPC

EC  
ITE  
**IT8528E**  
Package : LQPF128  
PAGE 35

PEG x 4 (port 5/6)

eDP (X2 lanes)

DDI

14" eDP Panel  
PAGE 26

HDMI CONN  
PAGE 27

PCIE Port 9

Giga LAN  
Realtek  
**RTL8111GUS**  
PAGE 28

RJ45  
PAGE 28

PCIE Port 6

USB2.0 Port 6

NGFF  
WLAN + BT  
PAGE 30

USB2.0 Port 4

Card Reader  
Realtek  
**RTS5176E**  
SD3.0  
DB

SD slot  
DB

USB2.0

Port 5  
Fingerprint  
PAGE 32

Port 7  
Camera  
PAGE 26

Port 8  
Touch Panel  
PAGE 26

USB3.0 port 1/2  
USB2.0 port 1/2

USB 3.0 port x2  
1 for power share  
TPS2546ARTER  
PAGE 30

USB3.0 port 3  
USB2.0 port 3

USB3.0 Re-driver  
PS8713B  
DB

USB 3.0 CONN  
Right  
DB

PAGE 2~16

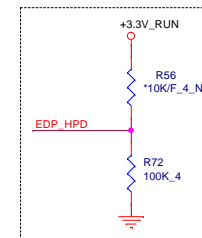
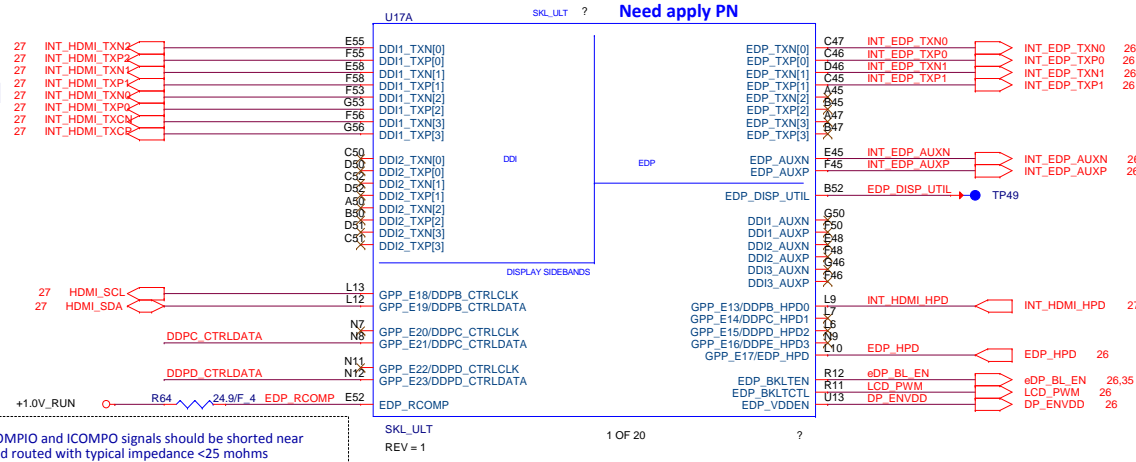


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PROJECT : AM8

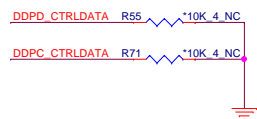
Size Document Number Rev  
BLOCK DIAGRAM 1A  
Date: Friday, May 22, 2015 Sheet 1 of 53

## HDMI



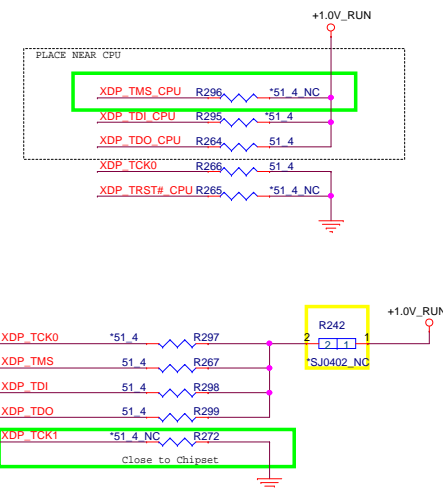
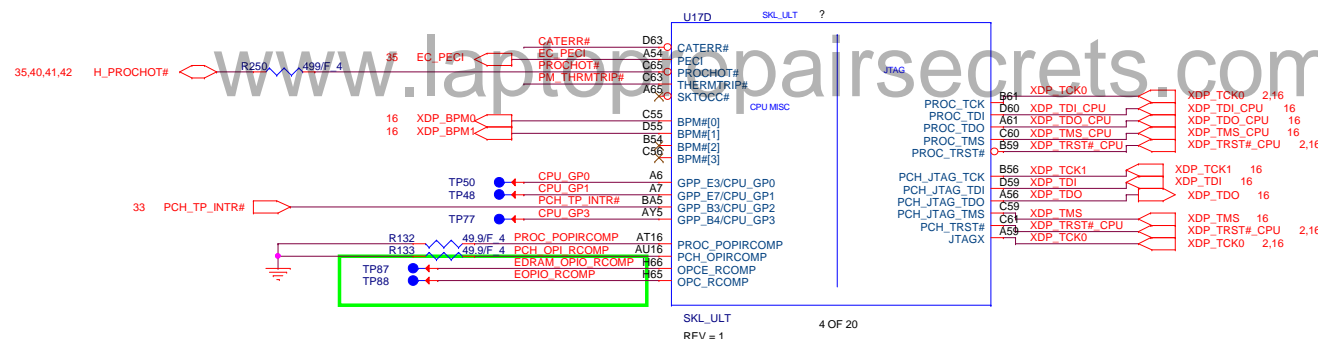
DDPB\_CTRLDATA/ GPP\_E19  
Display Port B Detected  
This signal has a weak internal pull-down.  
0 = Port B is not detected.  
1 = Port B is detected.

This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

DVT1 CPU P/N list	
AJ0QJFCUT04	CPU(1356P)SKL I3-6100U 2.3G QJFC WINCON
AJ0QJ8NUT04	CPU(1356P)SKL I5-6200U 2.3G QJ8N WINCON
AJ0QJ8LRT05	CPU(1356P)SKL I7-6500U 2.5G QJ8L WINCON



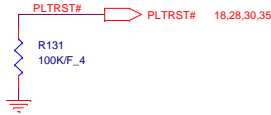
Close to EC



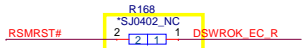
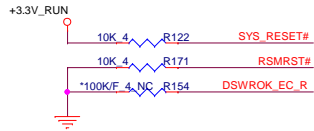
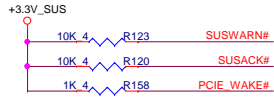
## SkyLake ULT Processor (DDR3L)



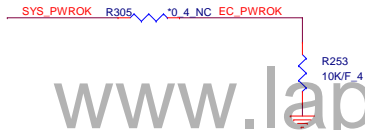
PLTRST#(CLG)



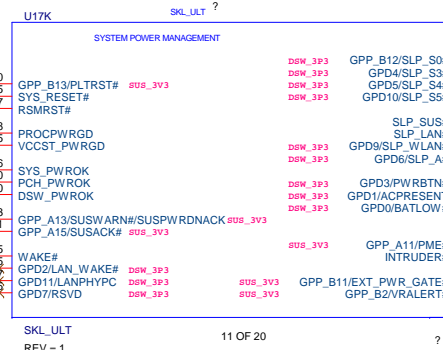
PCH Pull-high/low(CLG)



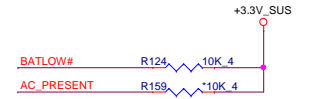
System PWR\_OK(CLG)

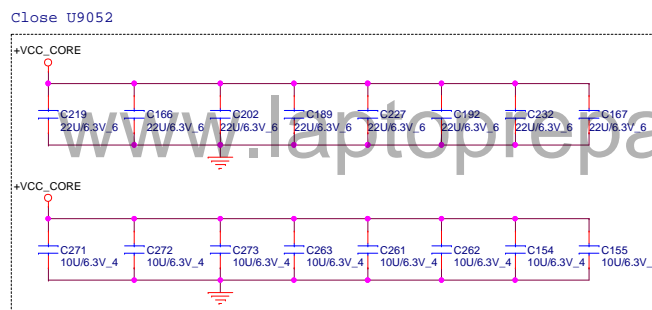
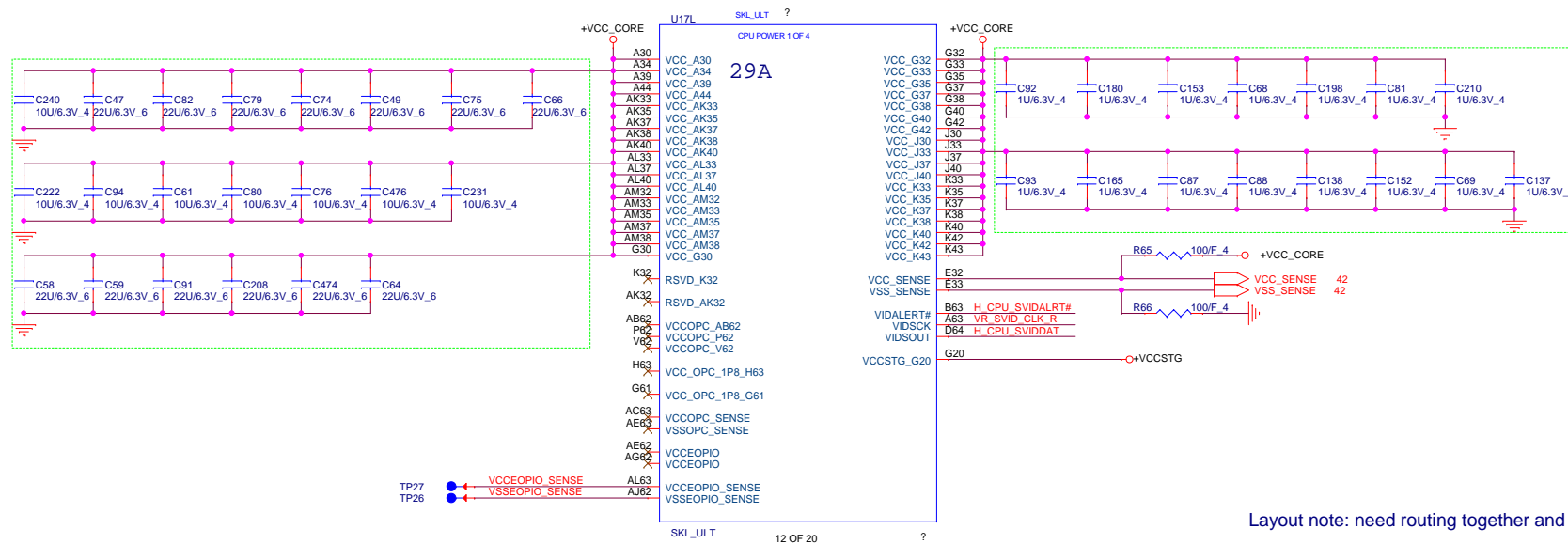


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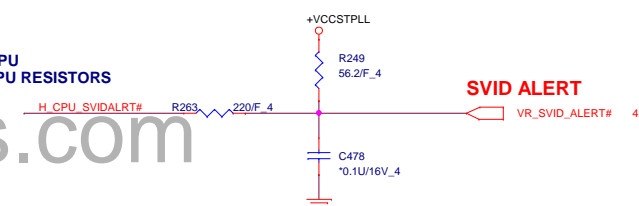
PCH Pull-high/low(CLG)



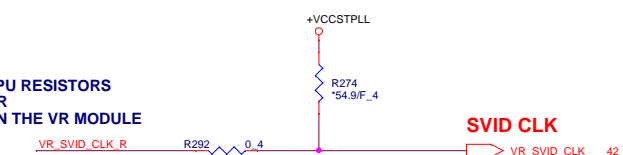


Layout note: need routing together and ALERT need between CLK and DATA.

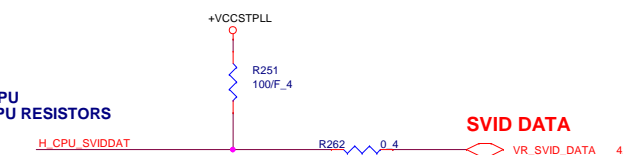
CLOSE TO CPU  
PLACE THE PU RESISTORS



PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



CLOSE TO CPU  
PLACE THE PU RESISTORS

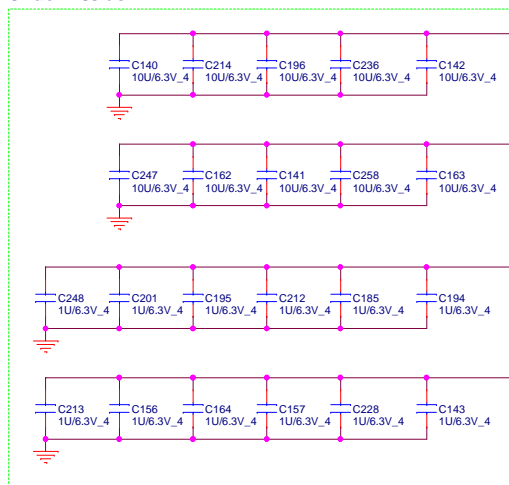


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
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V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1PB</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Under U9052

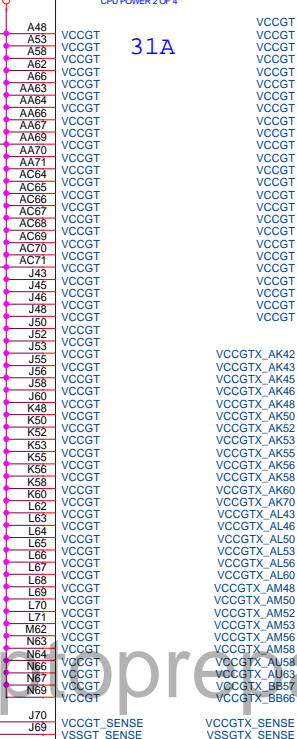


+VCCGT

U17M SKL\_ULT ?

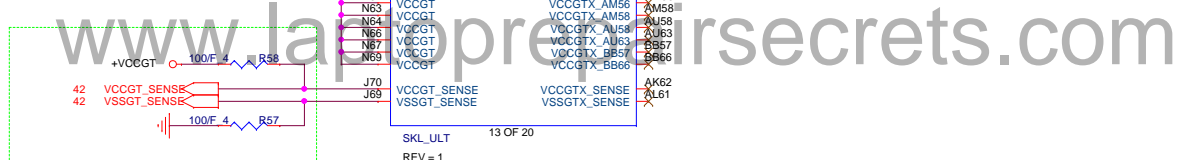
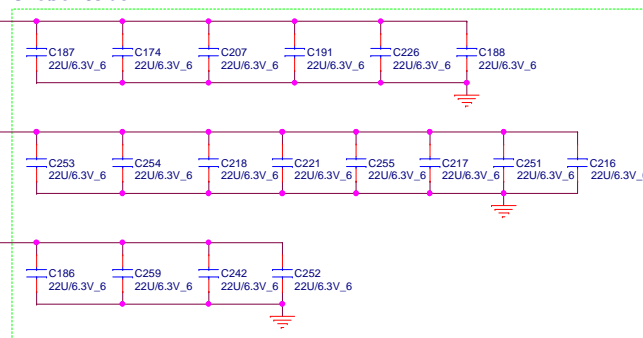
CPU POWER 2 OF 4

31A



+VCCGT

Close U9052



Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

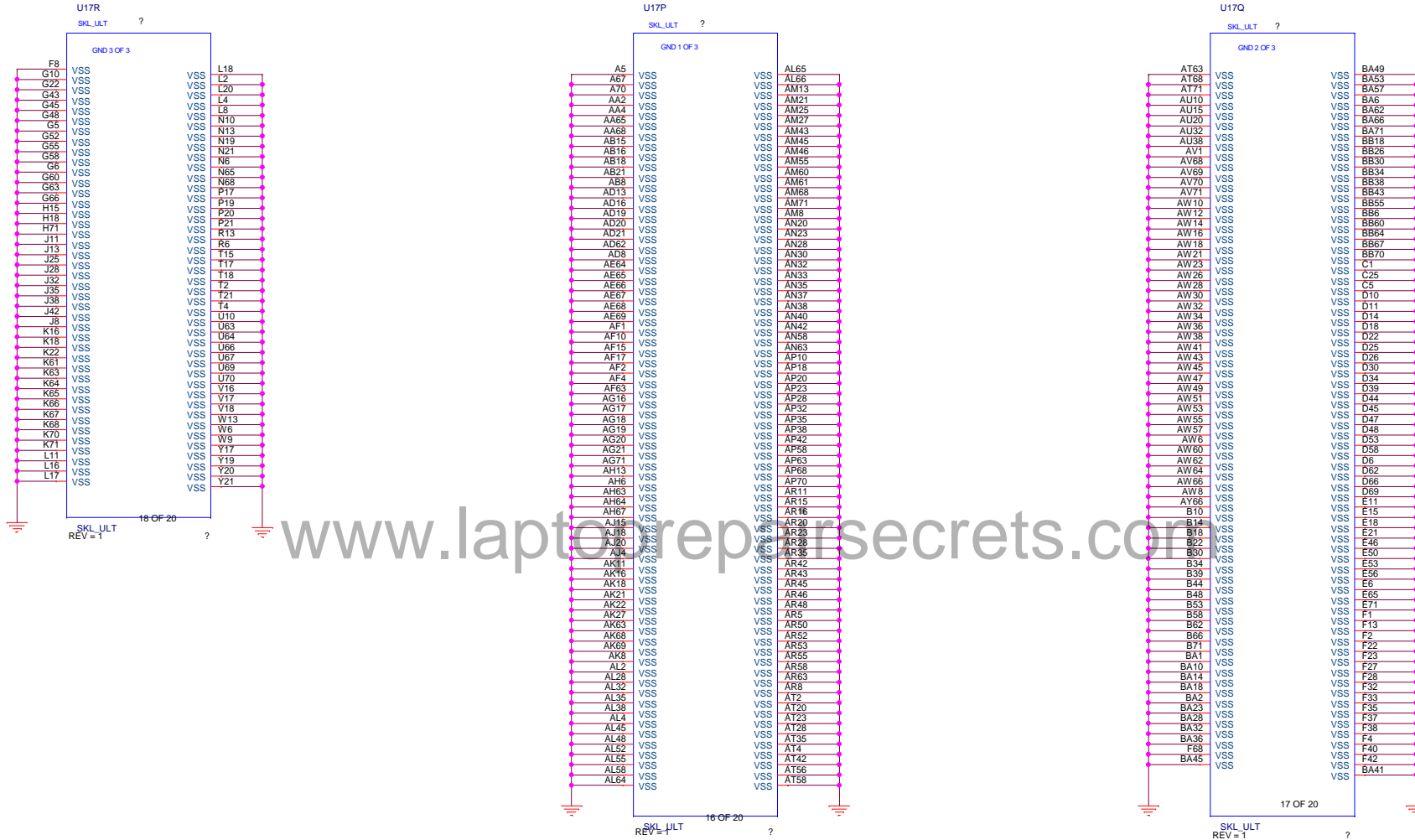
SKL\_ULT 13 OF 20  
REV = 1

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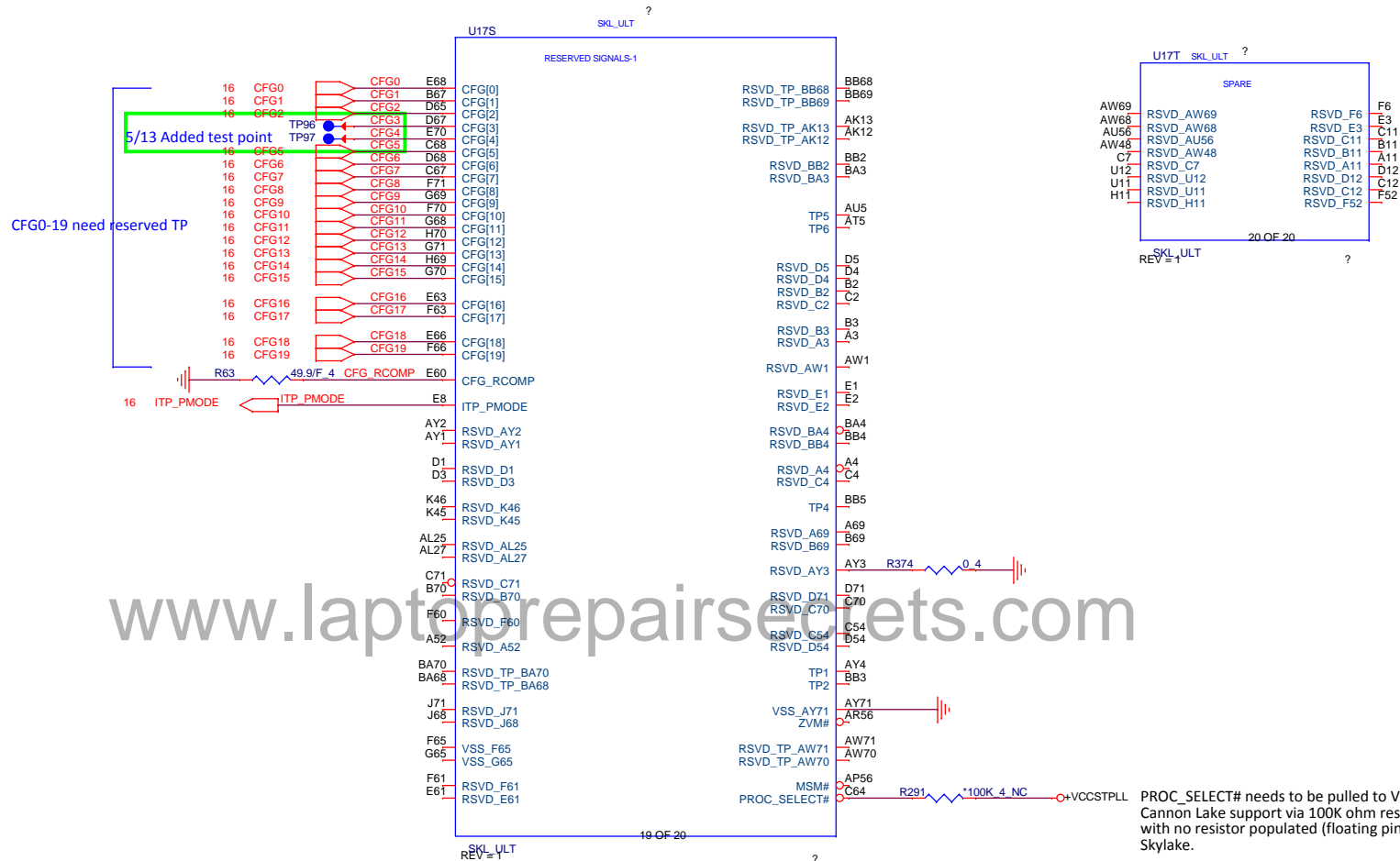
PROJECT : AM8

Size	Document Number	Rev
	SKL U 6/15 (POWER-3)	1A

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**Processor Strapping** The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

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PROJECT : AM8

Size

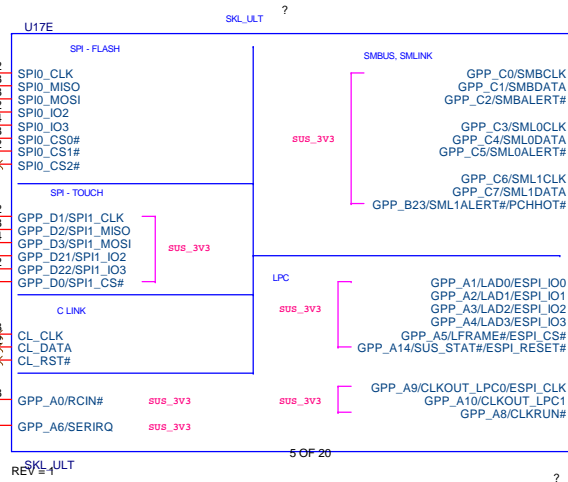
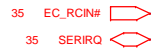
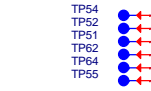
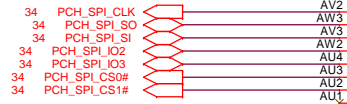
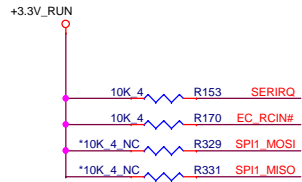
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**SKL U 8/15 (RSV)**

Date: Friday, May 22, 2015

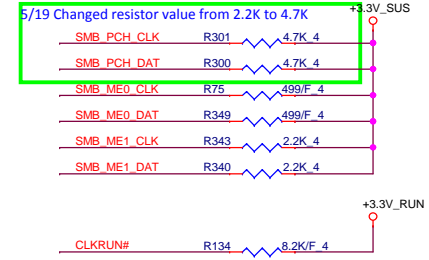
Rev  
1A

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## GPIO Pull UP

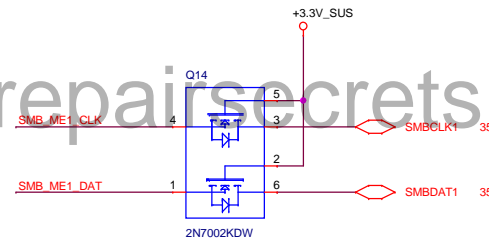


## GPIO Pull UP



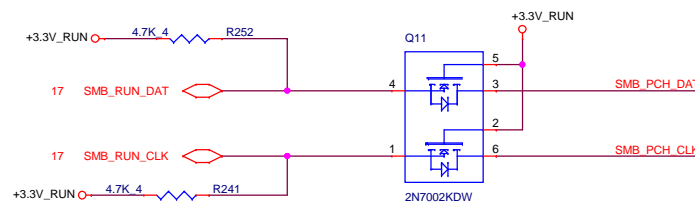
## SMBus/Pull-up(CLG)

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EC side

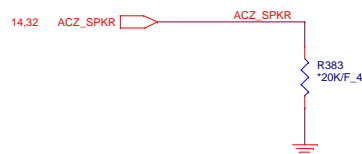
## XDP DDR3-L



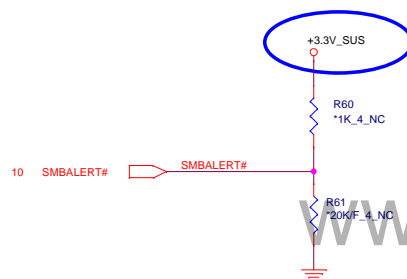
<b>Quanta Computer Inc.</b> <b>PROJECT : AM8</b>		
Size	Document Number	Rev
	<b>SKL U 9/15(SPI/LPC/SMBUS)</b>	<b>1A</b>
Date:	Friday, May 22, 2015	Sheet 10 of 53

# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET

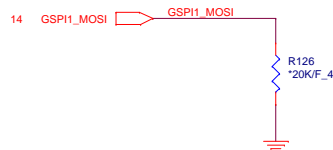


**Top-Block Swap Override:**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD

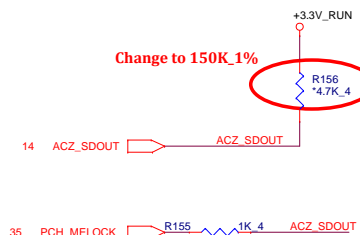


This signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

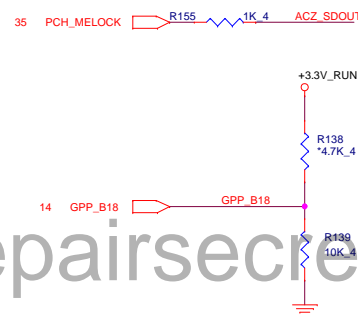
**Notes:**  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.



**BIOS Strap Bit(BBS):**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10      Boot BIOS Destination  
0            SPI  
1            LPC

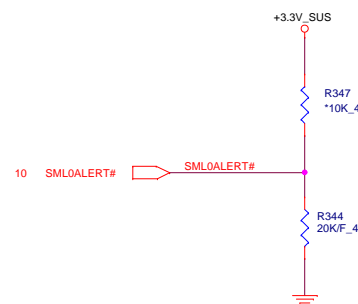


**Flash Descriptor Security Override:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



The signal has a weak internal pull-down.  
0 = Disable "No Reboot" mode. (Default)  
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

**Notes:**  
1. The internal pull-down is disabled after PLTRST# deasserts.  
2. This signal is in the primary well.



This signal has a weak internal pull-down.  
0 = LPC is selected for EC. (Default)  
1 = eSPI is selected for EC.

**Notes:**  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.

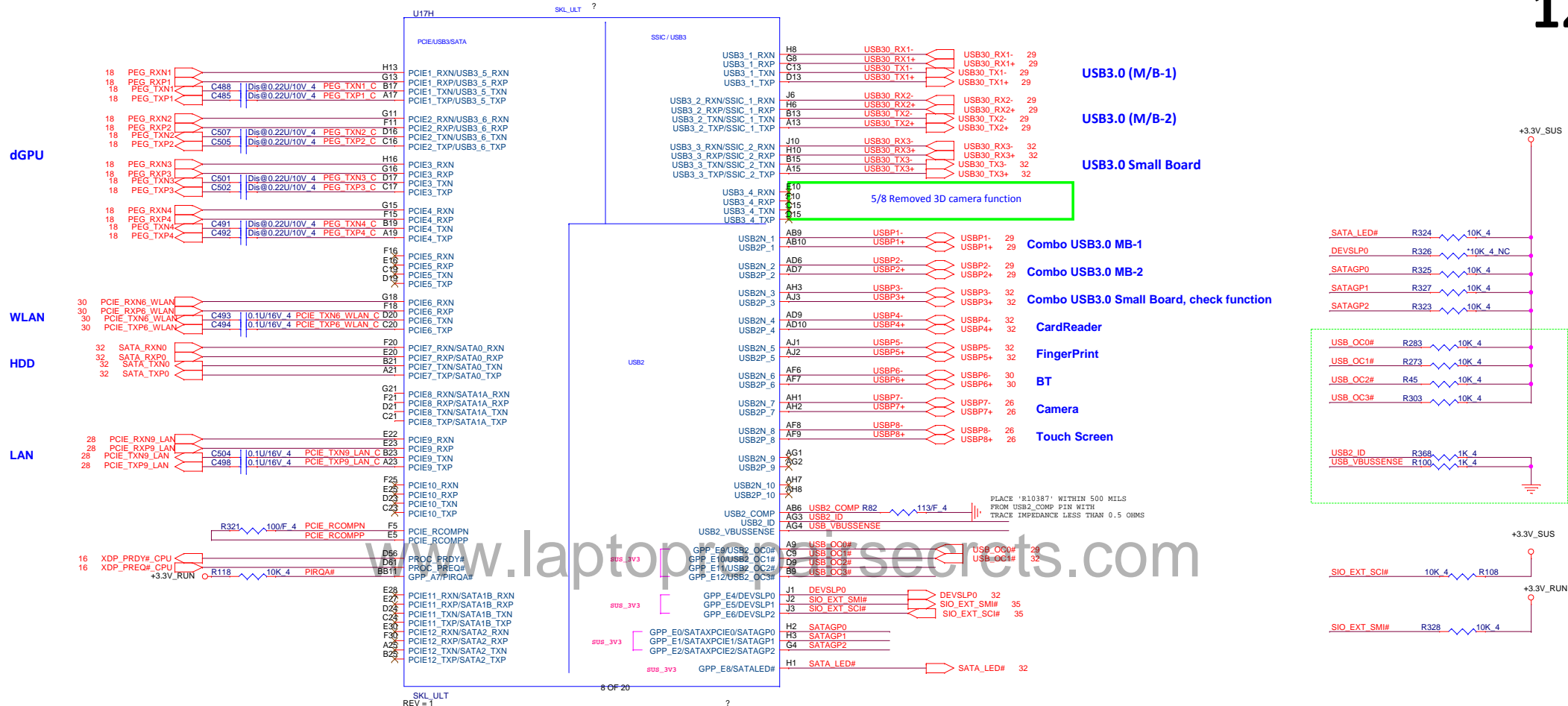


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**PROJECT : AM8**

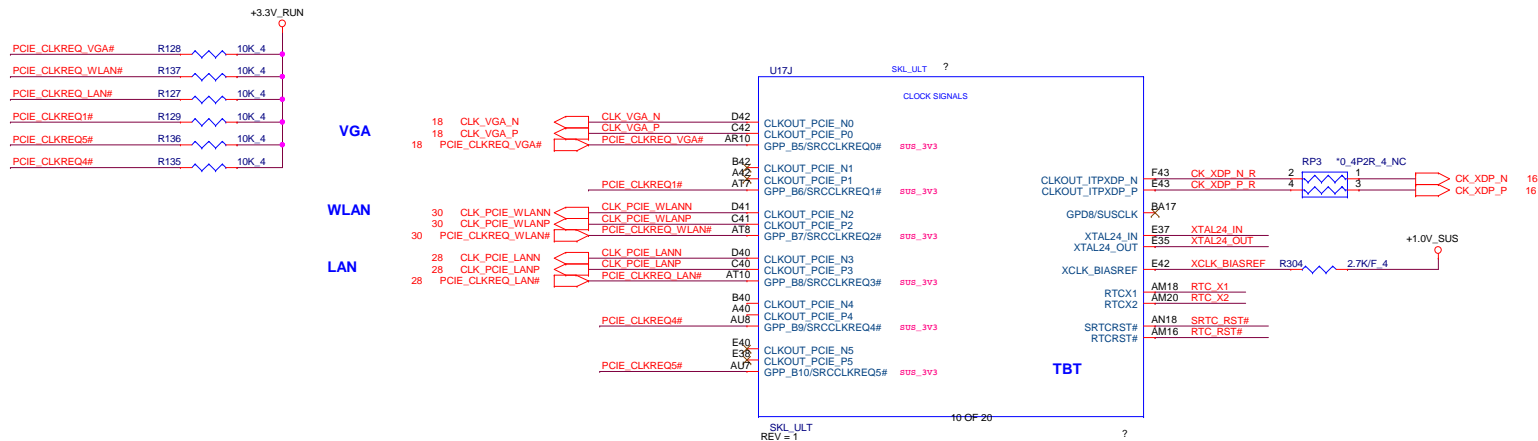
Size	Document Number	Rev
	<b>SKL U 10/15(HDA)</b>	<b>1A</b>

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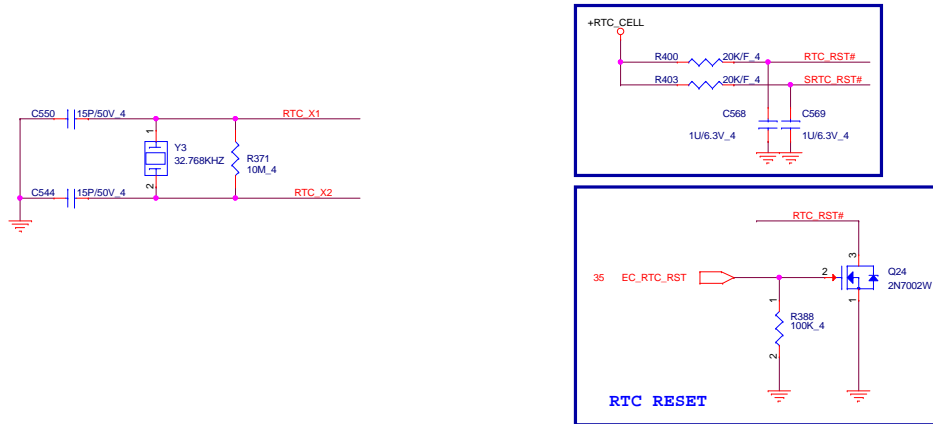
# CLK\_REQ/Strap Pin(CLG)

13

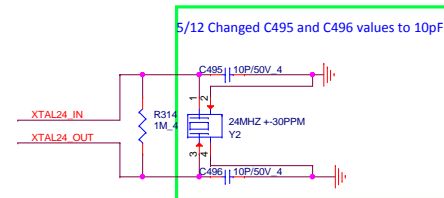


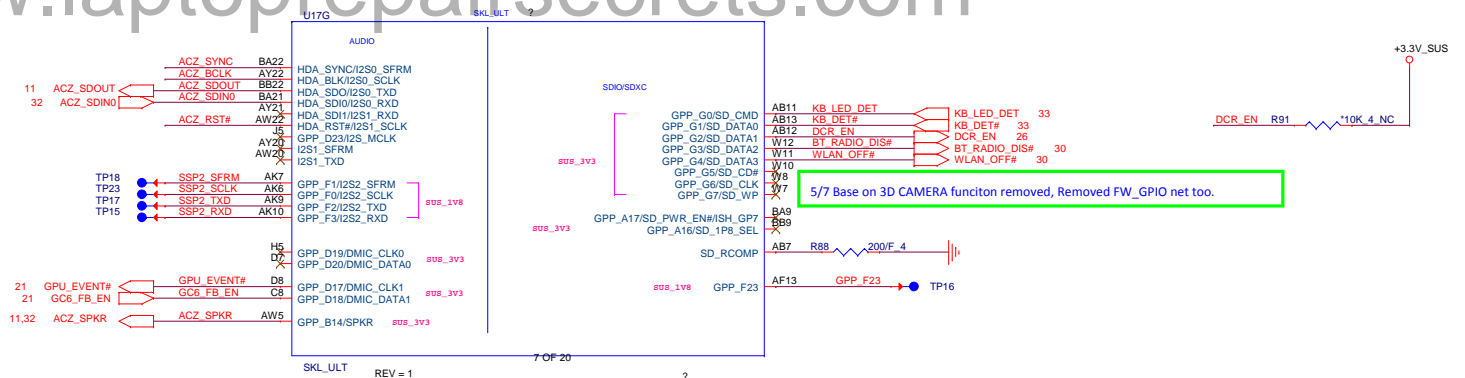
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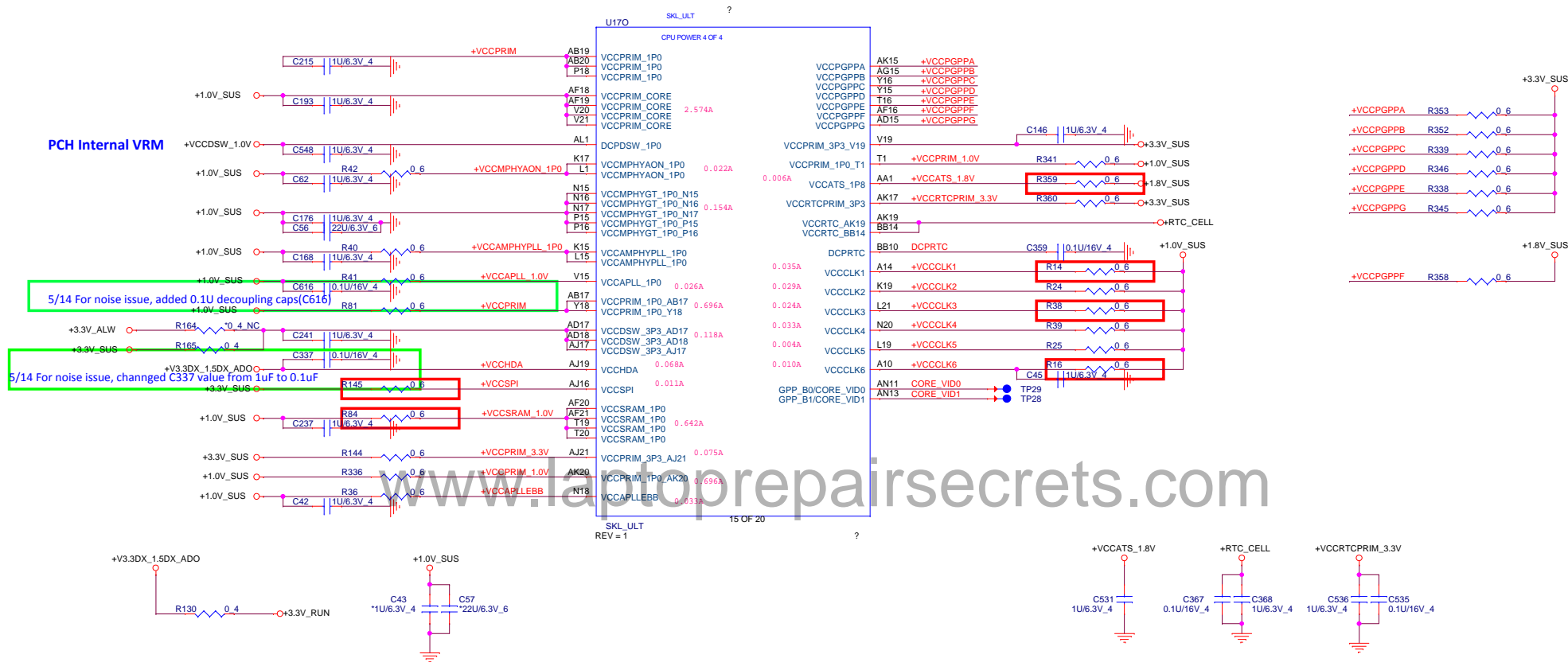
## RTC Clock 32.768KHz

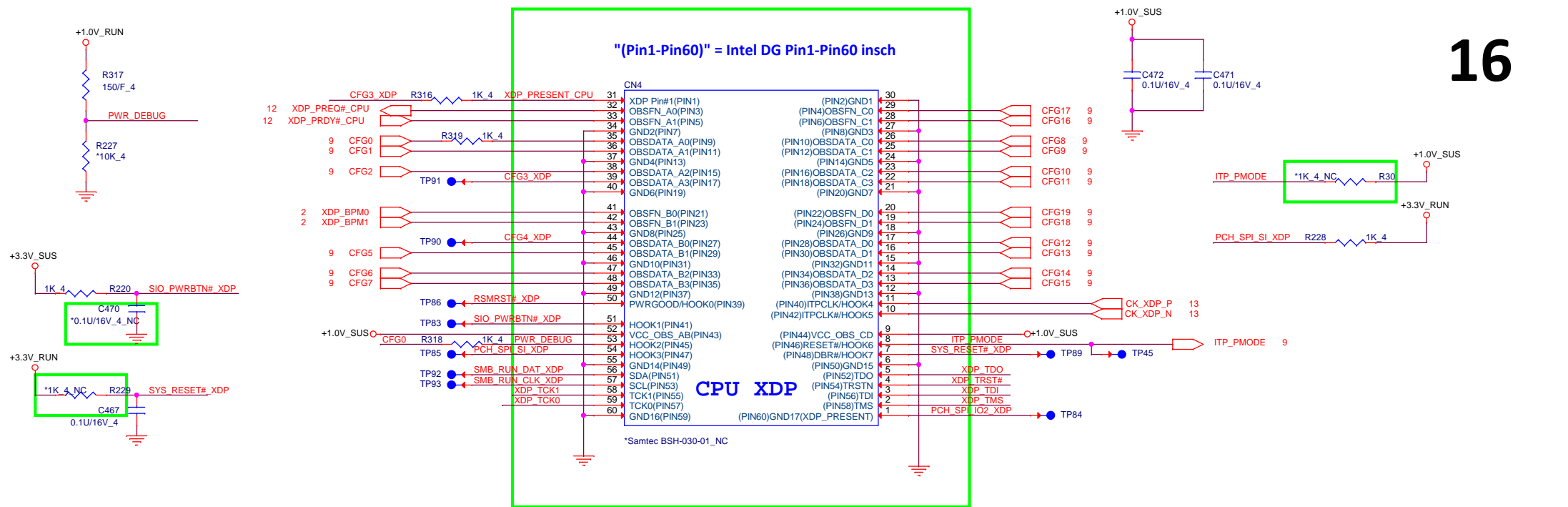


## External Crystal



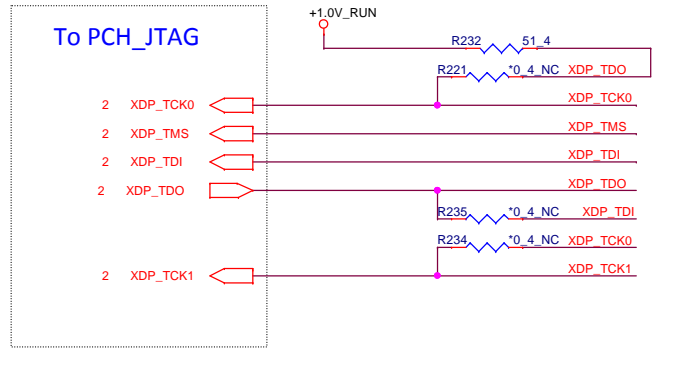






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5/14 Modified XDP schematic



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Size Document Number SKL U 15/15(XDP/APS\*) Rev 1A

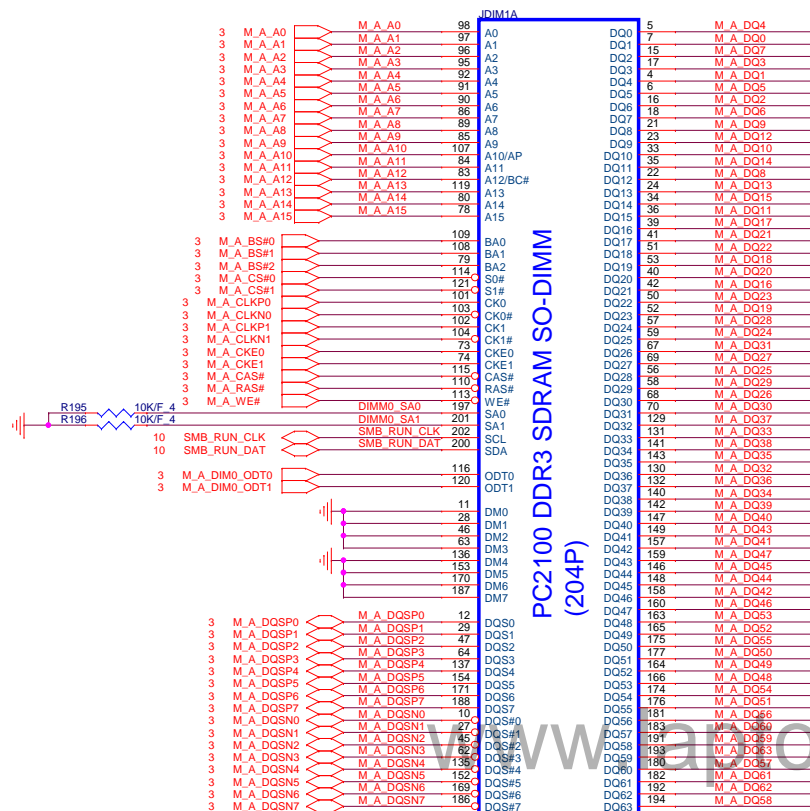
Date: Friday, May 22, 2015 Sheet 16 of 53



QP/N is DGMK4000412

M\_A\_DQ[63:0]

2.48A

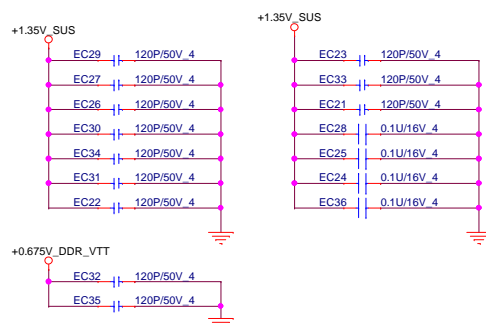


PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1, H=4.0\_RVS  
ddr-ds2rk-20401-tp4b-204p-ruv  
DGMK4000412

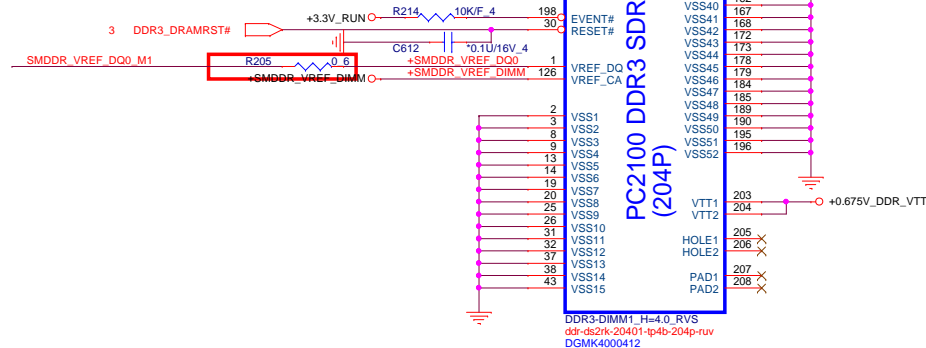
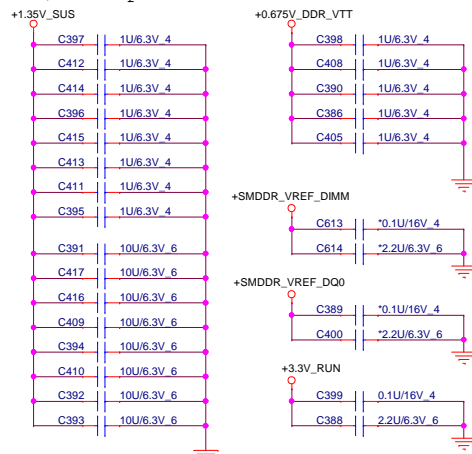
CPU Bracket

For EMI RESERVE

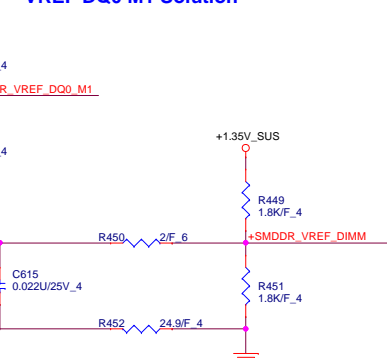


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

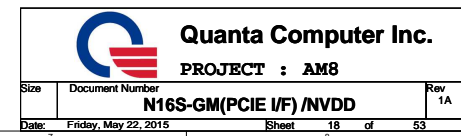


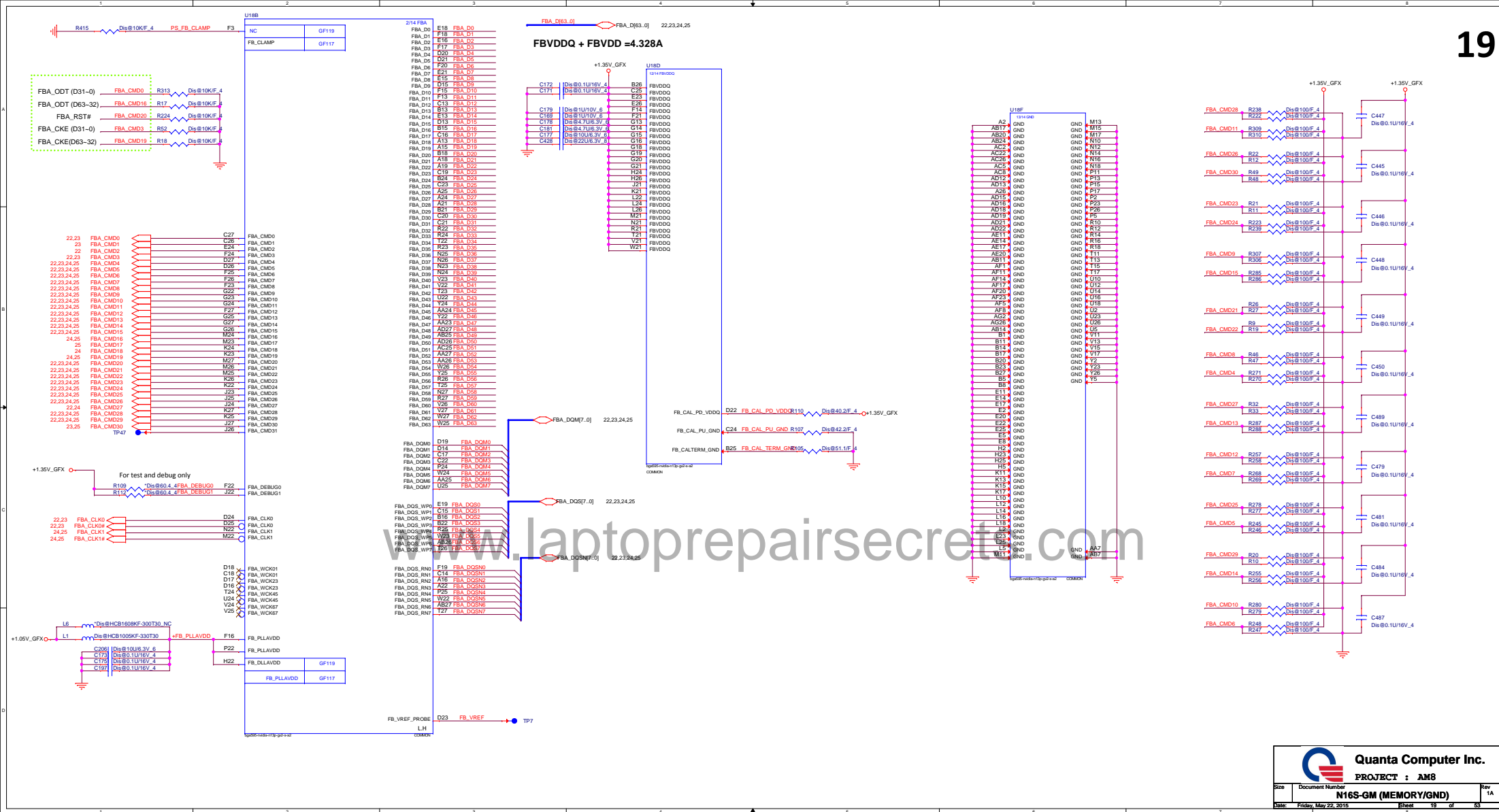
VREF DQ0 M1 Solution

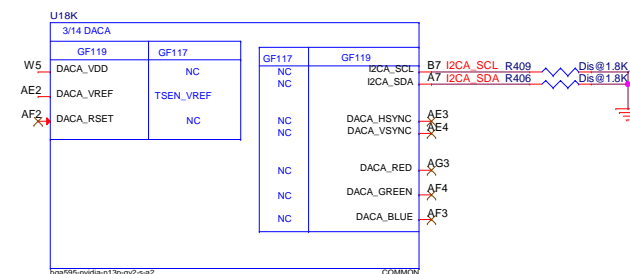
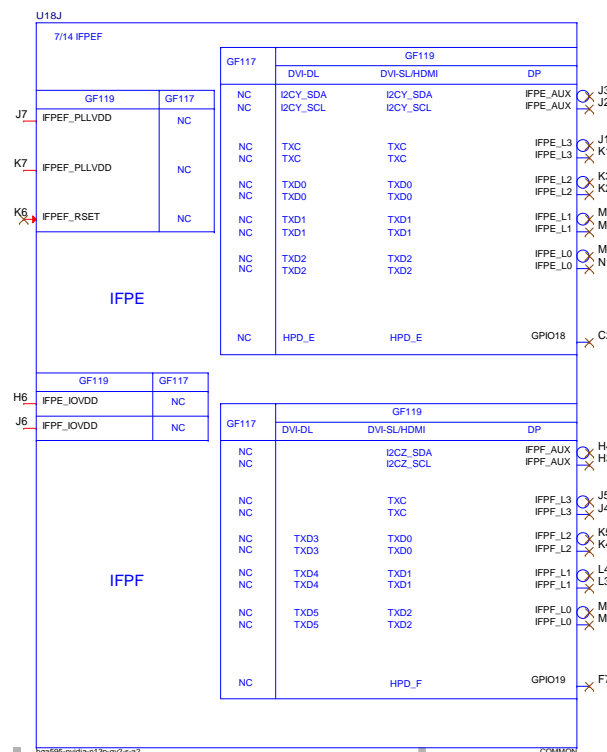
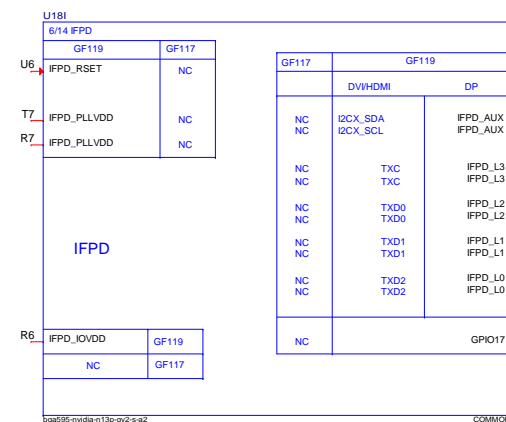
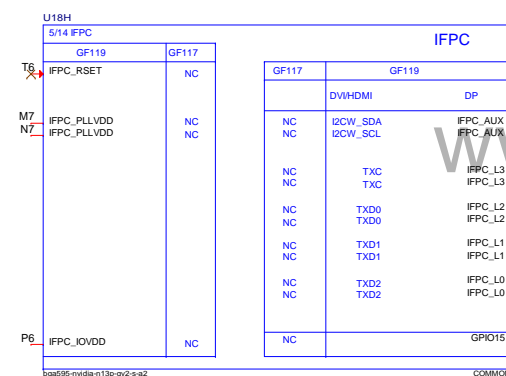
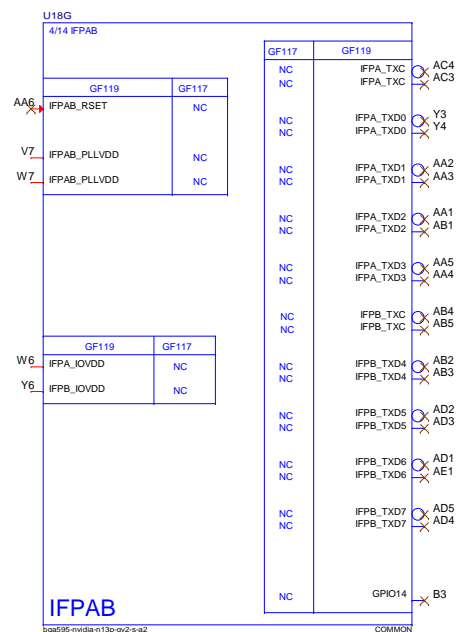


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Size Document Number  
DDR3 DIMM0-RVS(4.0H)  
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PLLVD = 38mA NC L3(0603,EOD) and populated L2(0402)

SP\_PLLVD = 17mA NC L5(0603) and populated L4(0402)

VID\_PLLVD = 41mA

XTAL SSIN

XTALIN

XTALOUT

XTALOUTBUFF

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

XTALOUT

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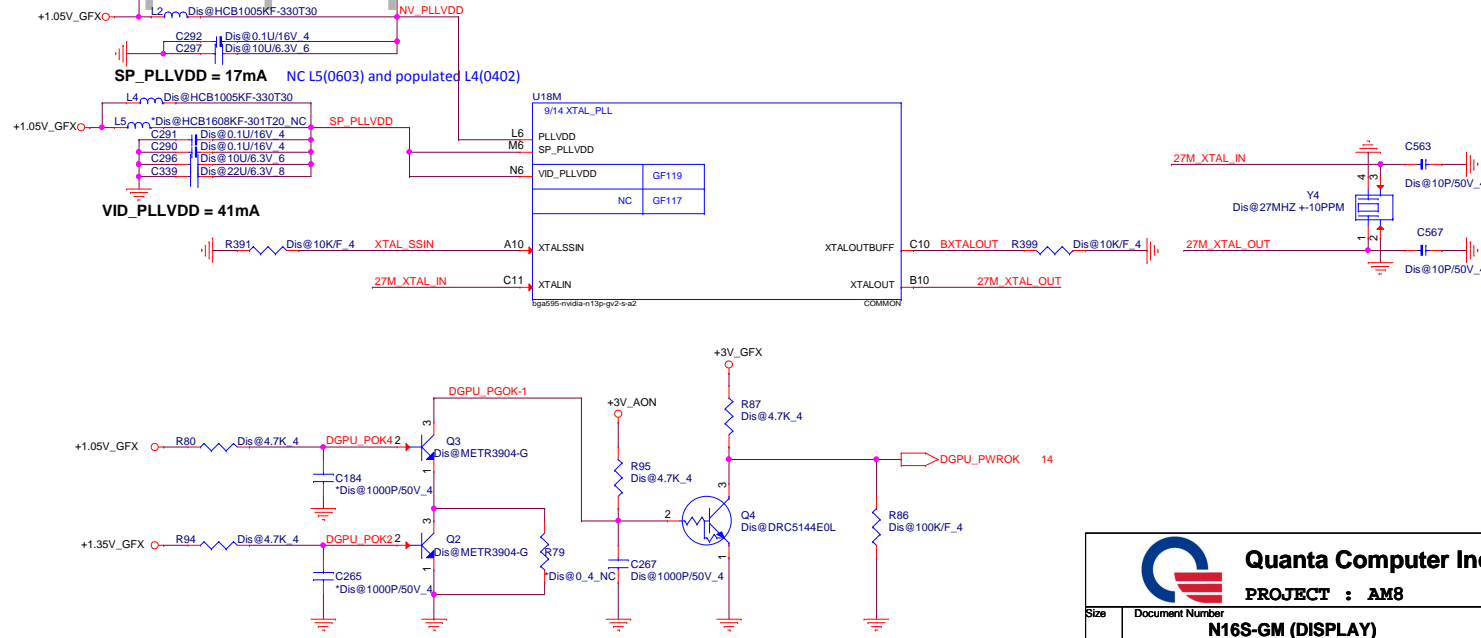
XTALOUT

XTALOUT

XTALOUT

XTALOUT

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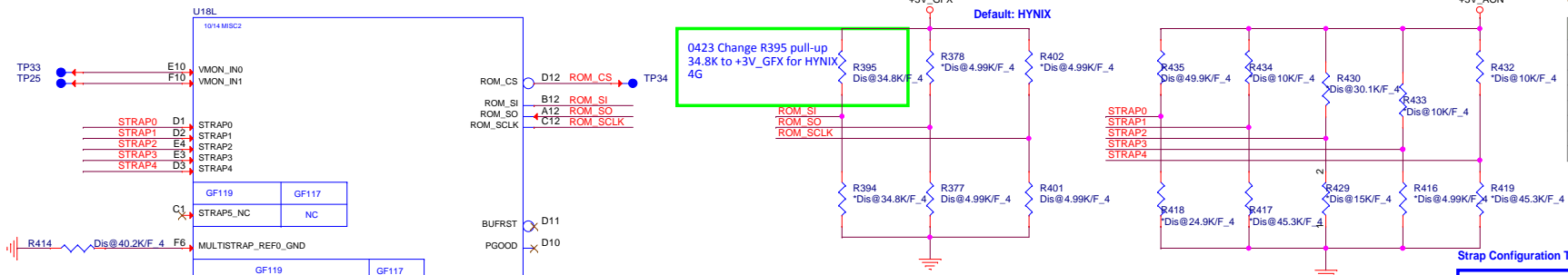


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99k CS24992PB26  
10k CS31002PB26  
15k CS31502PB24  
20k CS32002PB29  
24.9k CS32492PB16  
30.1k CS33012PB18  
34.8k CS33482PB22  
45.3k CS34532PB18

Strap Configuration Table

Strap Pin	Strap Mapping	Resistance	Note
ROM_SCLK	SOR3_EXPOSED SOR2_EXPOSED SOR1_EXPOSED SOR0_EXPOSED	5Kohm, L	
ROM_SI	RAM_CFG[3] RAM_CFG[2] RAM_CFG[1] RAM_CFG[0]	10Kohm, L 45Kohm, H 25Kohm, L 30Kohm, H 15Kohm, L 35Kohm, H	0001 -> SAM (S.R.) 1111 -> SAM (D.R.) 0100 -> Micron (S.R.) 1101 -> Micron (D.R.) 0010 -> Hynix (S.R.) 1110 -> Hynix (D.R.)
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGA_DEVICE	5Kohm, L	0000
STRAP0	Keep pull-up to +3.3V_ON & pull-down to GND footprint, and stuff 50K pull-up		
STRAP1 STRAP2 STRAP3 STRAP4	RESERVED		

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	DELL P/N	QCI P/N
0001 0x1 1111 0xF	K4W4G1646E-BC1A	SAMSUNG	NA	AKD5PGDT502
0100 0x4 1101 0xD	MT41J256M16HA-093G:E	Micron	NA	AKD5PZSTL02
0010 0x2 1110 0xE	H5TC4G63CFR-N0C	Hynix	NA	AKD5PZDTW00

## GPIO ASSIGNMENTS ( GB2B-64 )

Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GC6_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



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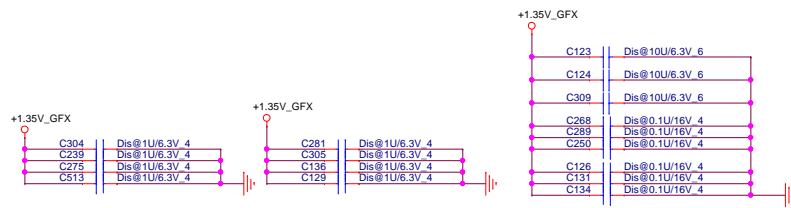
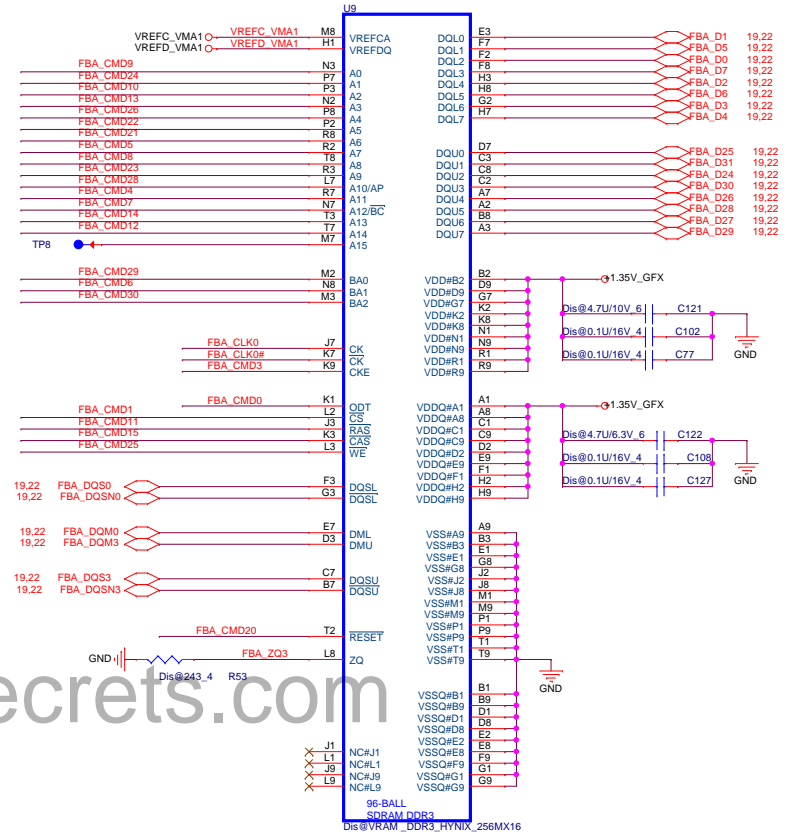
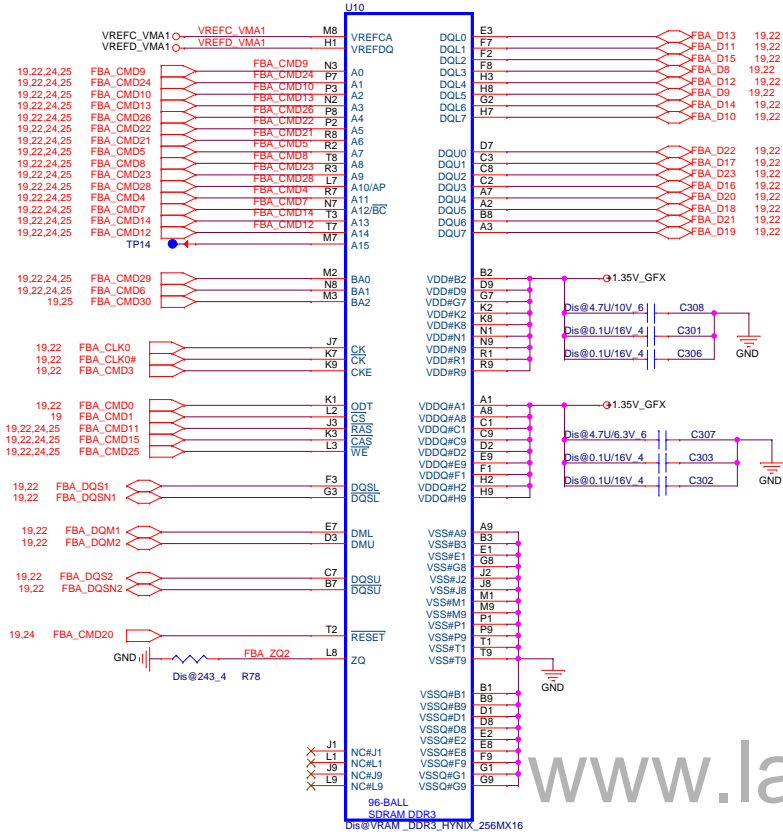
N16S-GM (GPIO/STRAPS)

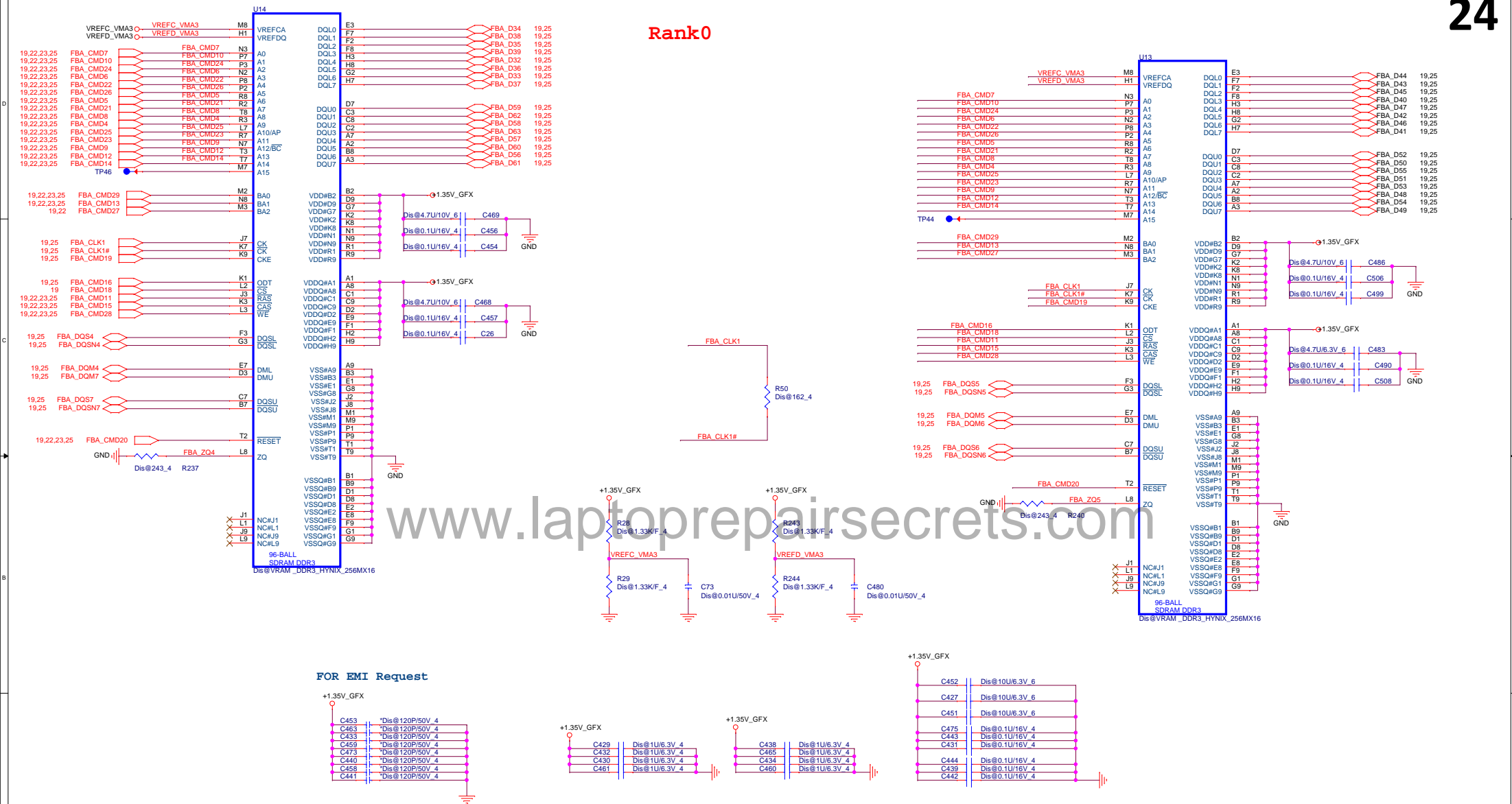
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Rank1





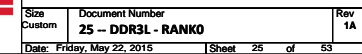
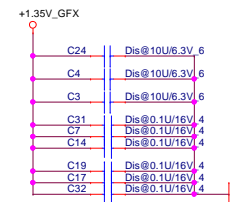
**Quanta Computer Inc.**  
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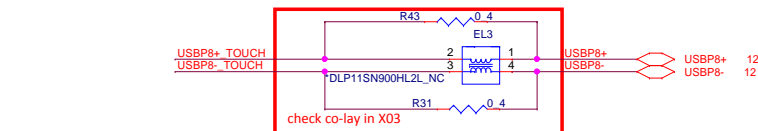
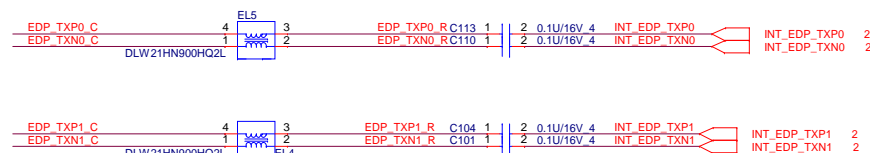
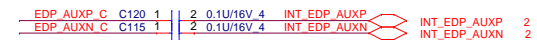
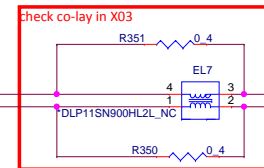
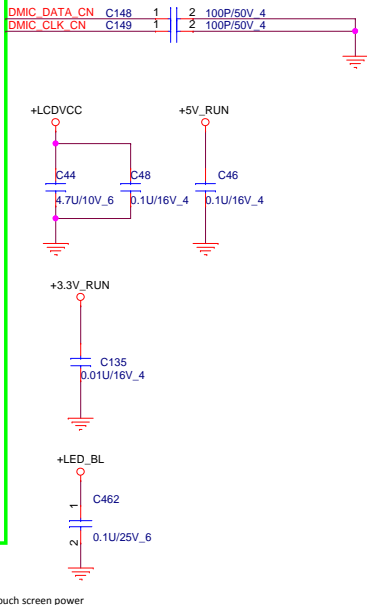
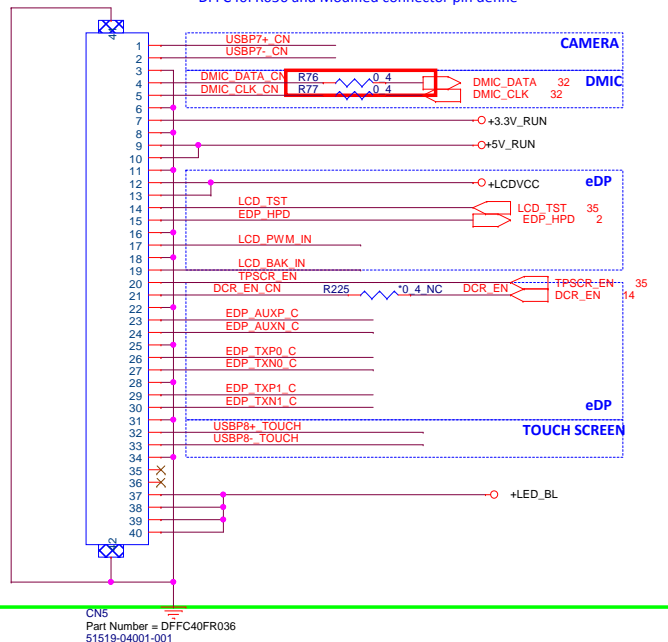


## +1.35V\_GFX



### eDP CONN(LDS)

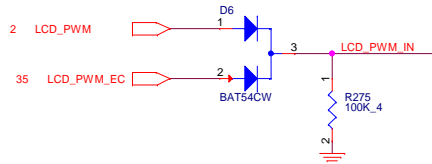
5/8 Changed LVDS conn from 50 pin to 40 pin, P/N use DFFC40FR036 and Modified connector pin define



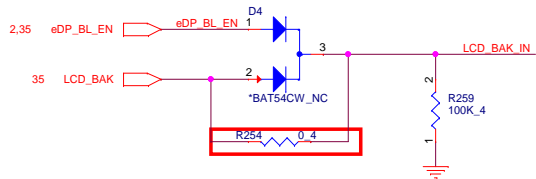
5/7 Removed 3D camera function

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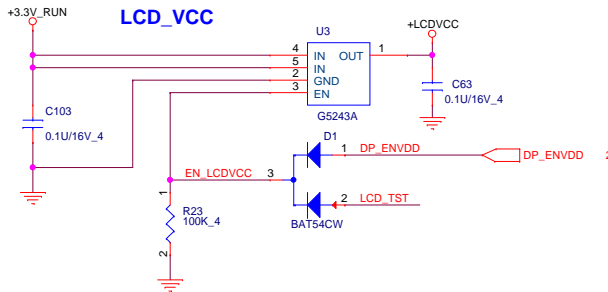
### Backlight Control(LDS)



### Backlight Enable(LDS)



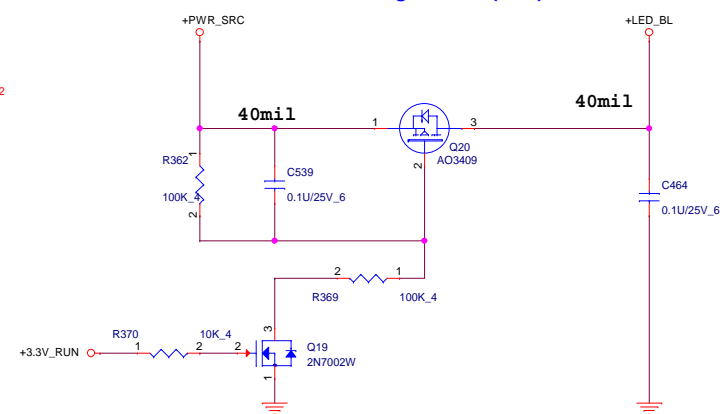
### LCD\_VCC



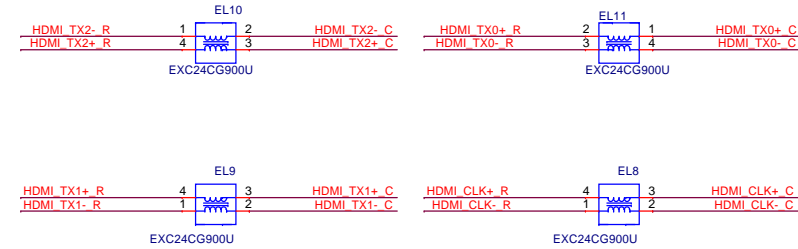
### 3D CAMERA Power

5/7 NC 3D camera power schematic

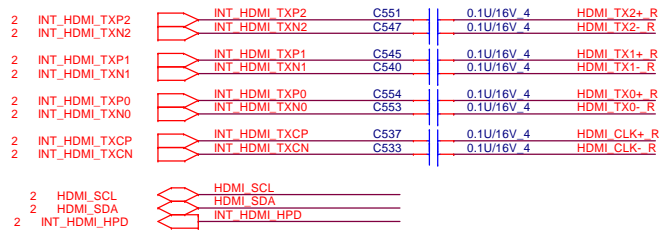
### Backlight Power(LDS)



Reserve for EMI and close to HDMI CONN(EMC)

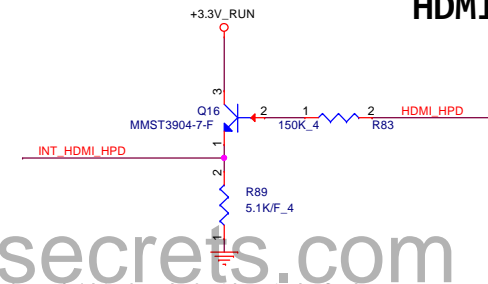


## HDMI (HDM)



HDMI\_HPD spec VinH\_min=2.0V

## HDMI HPD



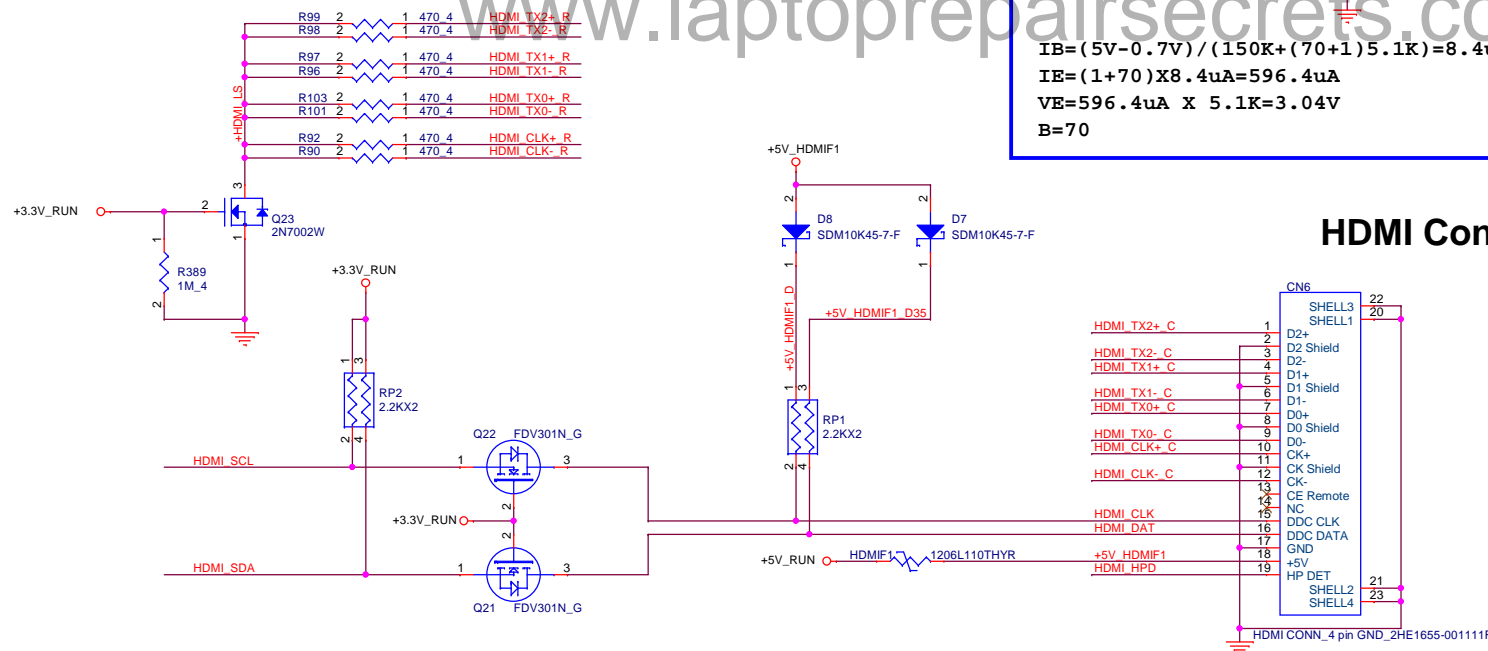
$$IB = (5V - 0.7V) / (150K + (70 + 1)5.1K) = 8.4\mu A$$

$$IE = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$VE = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$

## HDMI Conn.(HDM)



0213 HDMI connector used DFHD19MR249

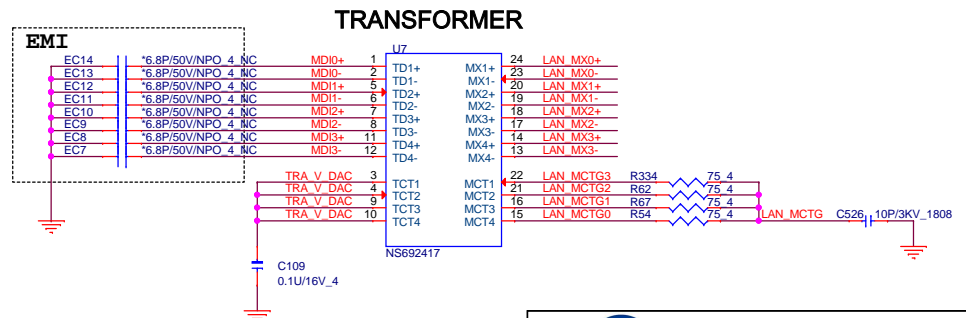
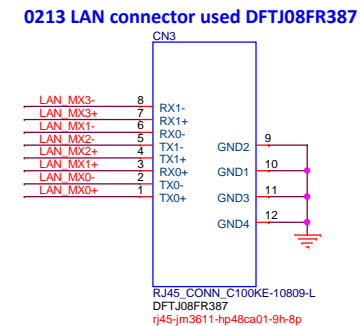
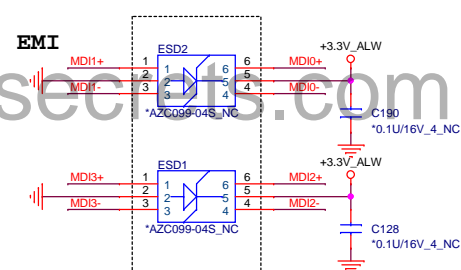
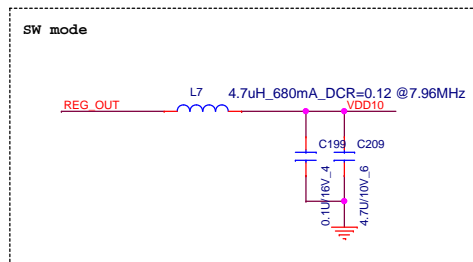
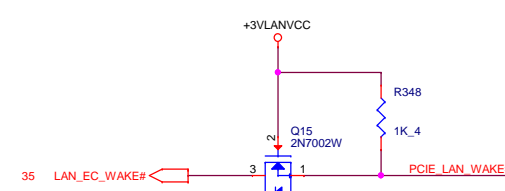
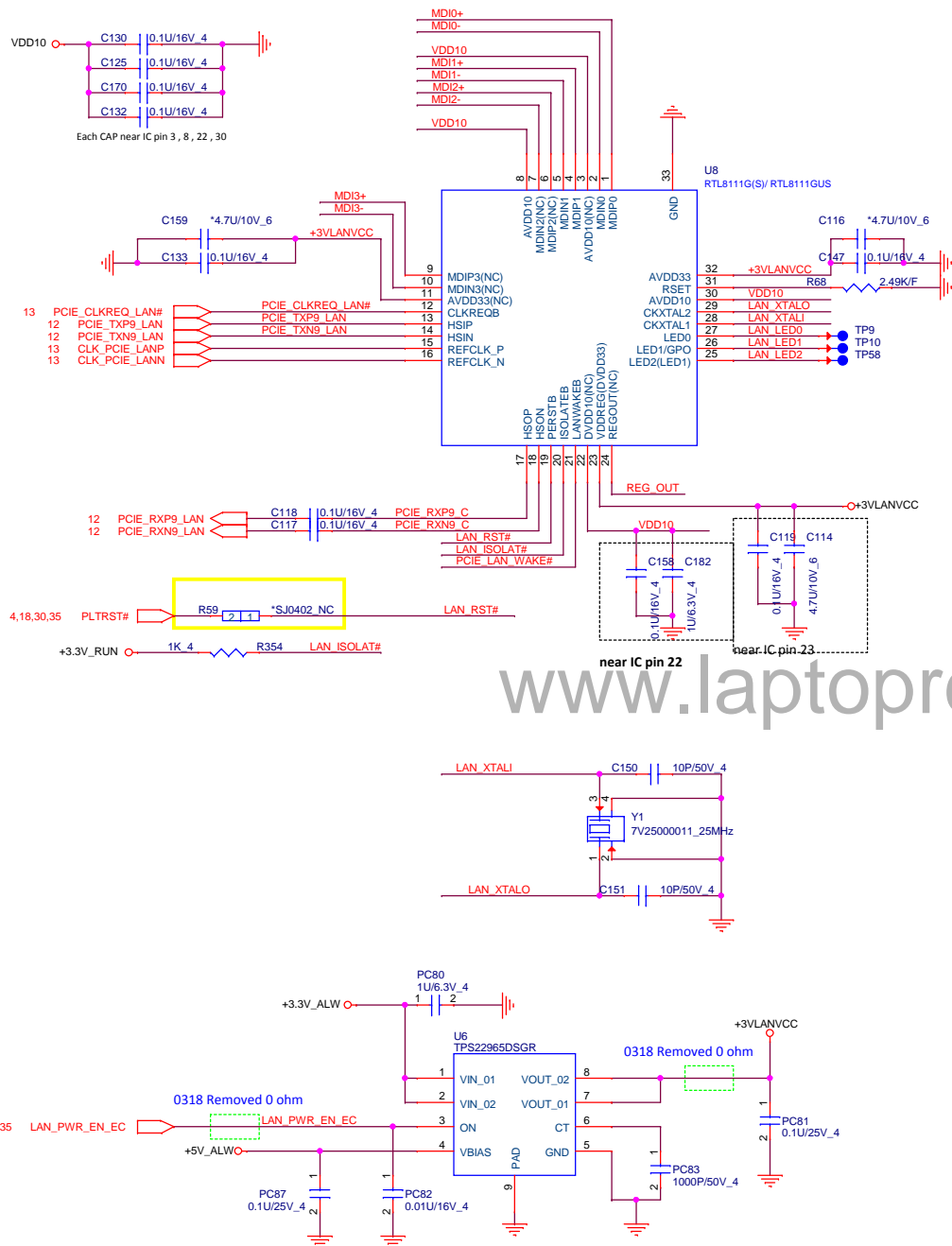


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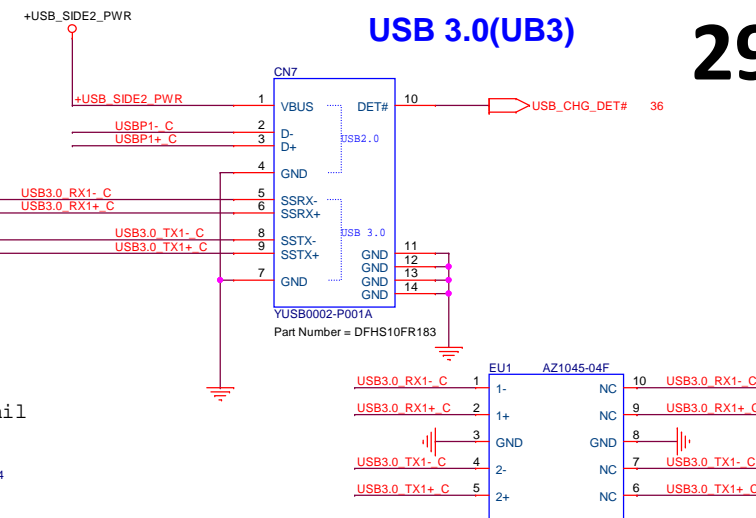
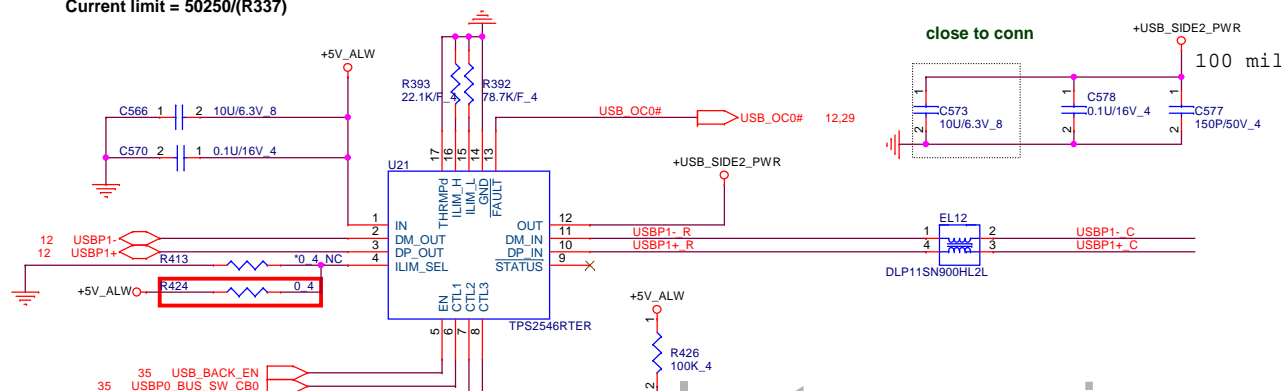
HDMI CONN

# LAN RTL8111GUS-CG (LAN)

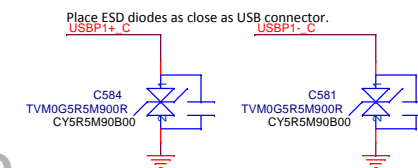


## 29

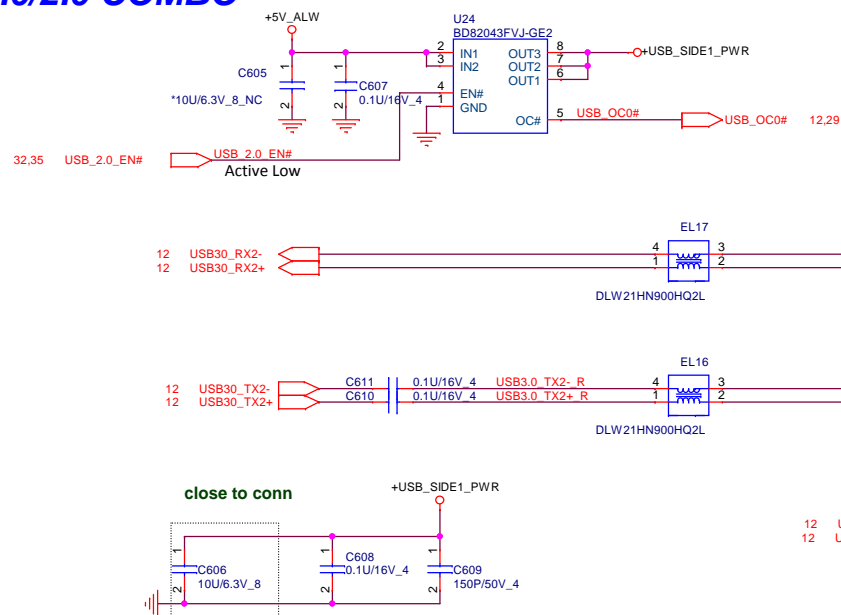
**Current limit = 50250/(R337)**



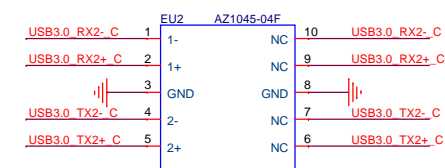
## ESD Function



**M15 Design Requirement:**  
**I continuous 1.5A ; OC 2.0A**

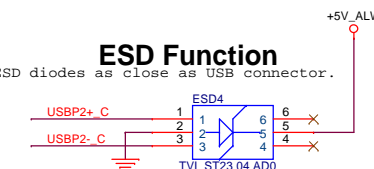


PUBAUU-09FLBS1NN4H0  
Part Number = DFHS09FR667



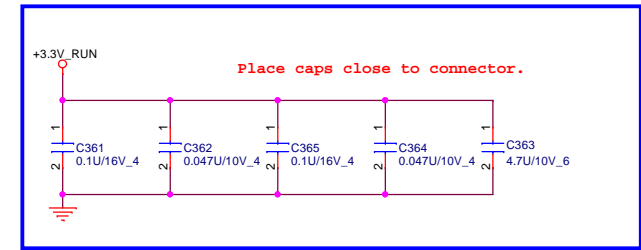
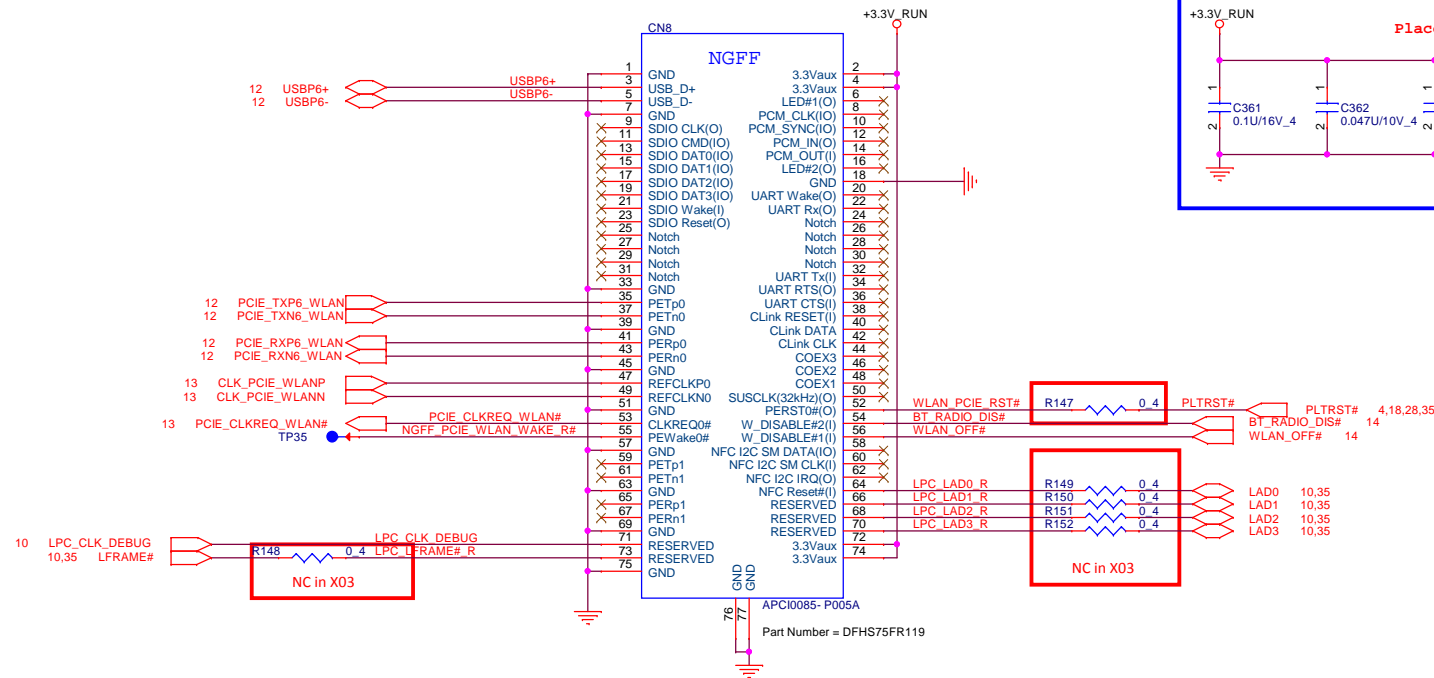
## ESD Function

Place ESD diodes as close as USB connector.



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	<b>USB3/USB Charger</b>	
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# NGFF Wifi/BT connector(NGF)



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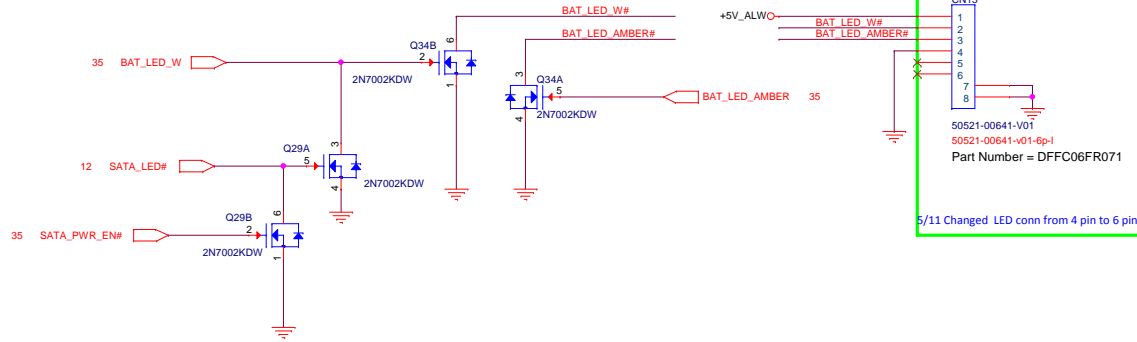
Size	Document Number	Rev
	Wifi/BT NGFF	1A
Date:	Friday, May 22, 2015	Sheet 30 of 53

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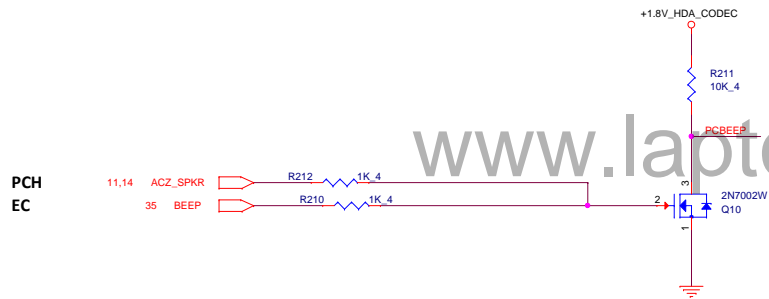
		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : AM8</b>	
Size	Document Number	Rev 1A	
<b>USB3.0 Redriver</b>			
Date:	Friday, May 22, 2015	Sheet	31 of 53

## TO LED DB

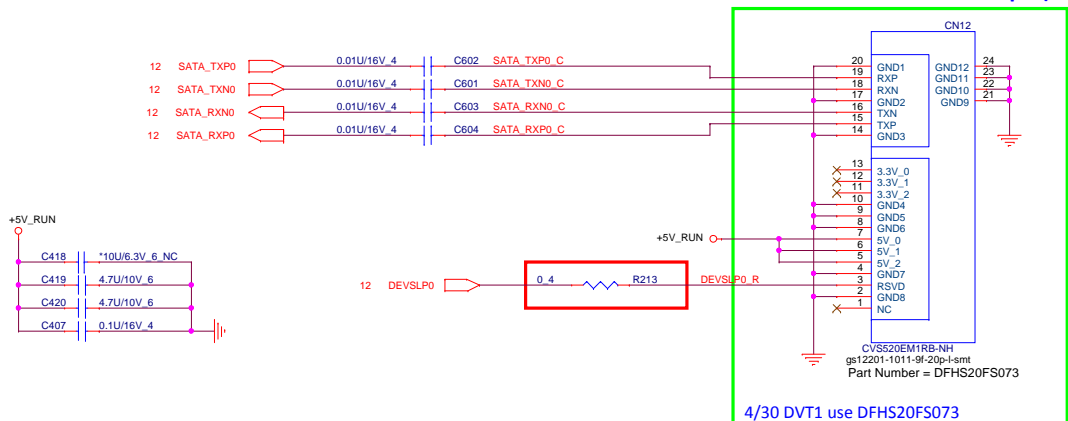
## Charger LED (UIF)



## To Small Board Codec BEEP function (ADO)

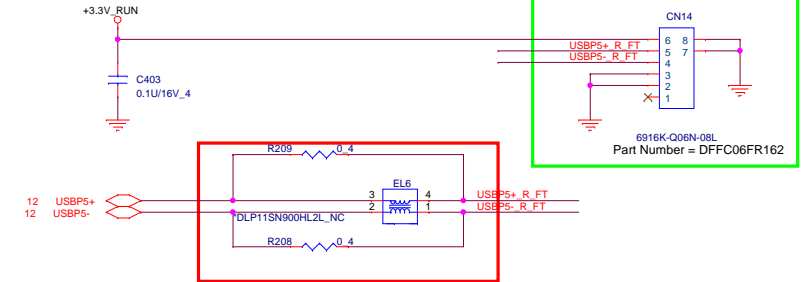


## SATA HDD Connector 20pin(HDD)



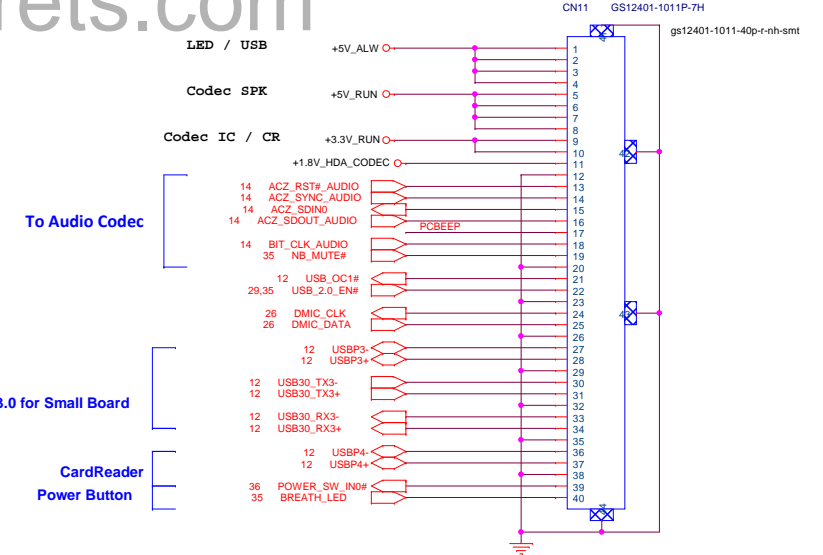
## Fingerprint(FPD)

5/8 Modified connector pin define



## TO DB Connector

Part Number = DFHS40FS036

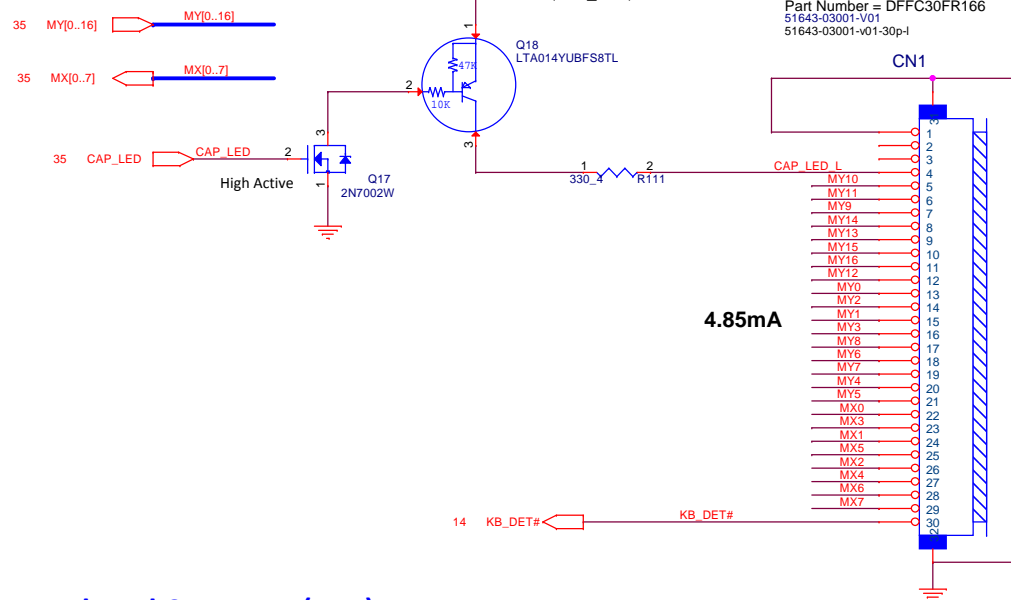


## Combo USB3.0 for Small Board

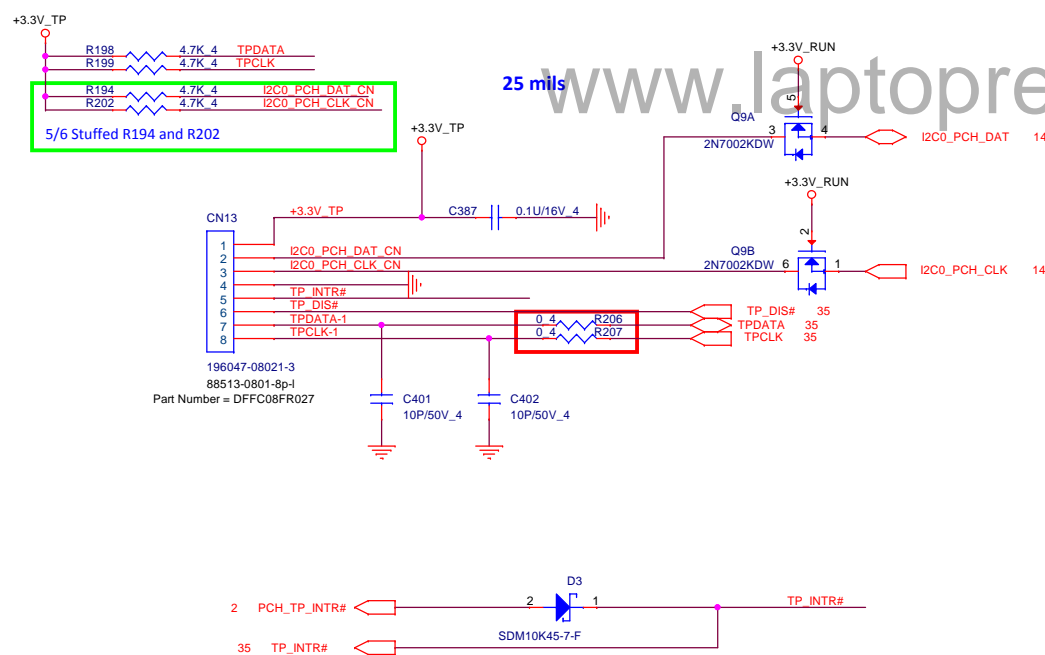
CardReader  
Power Button



Keyboard Connector(KBC)



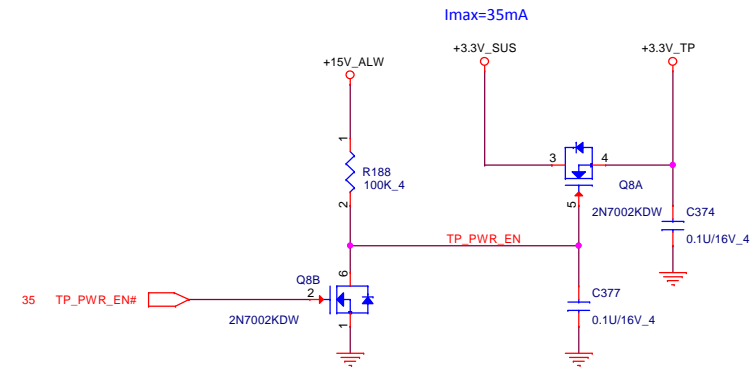
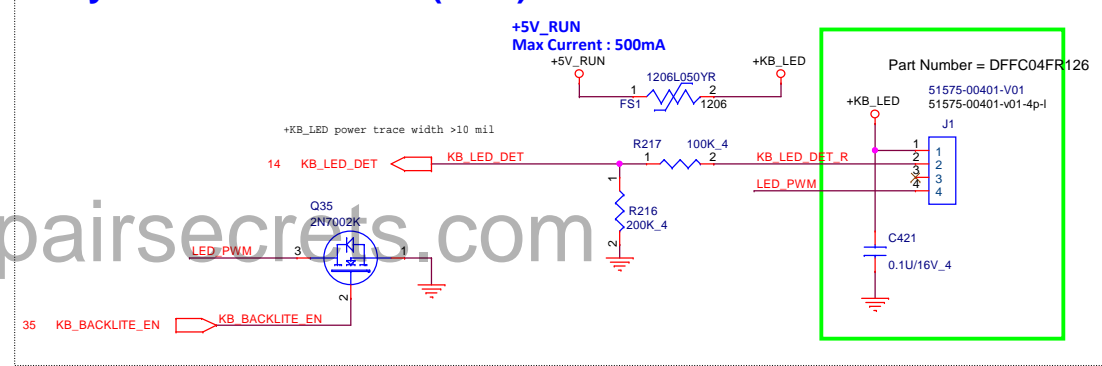
Touch Pad Connector(TPD)



MY1	C323	1	2	100P/50V_4
MY2	C322	1	2	100P/50V_4
MY4	C328	1	2	100P/50V_4
MY0	C321	1	2	100P/50V_4
MX4	C312	1	2	100P/50V_4
MX6	C335	1	2	100P/50V_4
MX3	C331	1	2	100P/50V_4
MX2	C334	1	2	100P/50V_4
MY5	C329	1	2	100P/50V_4
MY6	C326	1	2	100P/50V_4
MY3	C324	1	2	100P/50V_4
MY7	C327	1	2	100P/50V_4
MY8	C325	1	2	100P/50V_4
MY9	C315	1	2	100P/50V_4
MY10	C313	1	2	100P/50V_4
MY11	C314	1	2	100P/50V_4
MX7	C311	1	2	100P/50V_4
MX0	C330	1	2	100P/50V_4
MX5	C333	1	2	100P/50V_4
MX1	C332	1	2	100P/50V_4
MY12	C320	1	2	100P/50V_4
MY13	C317	1	2	100P/50V_4
MY14	C316	1	2	100P/50V_4
MY15	C318	1	2	100P/50V_4
MY16	C319	1	2	100P/50V_4

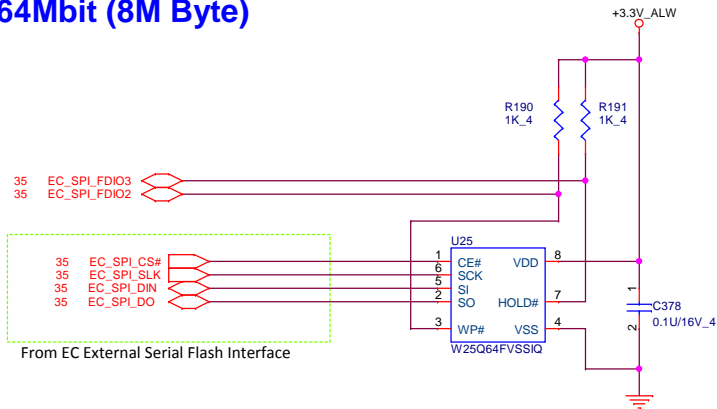
Key board illumination(KBL)

4/23 changed KB BL connector P/N to DFFC04FR126



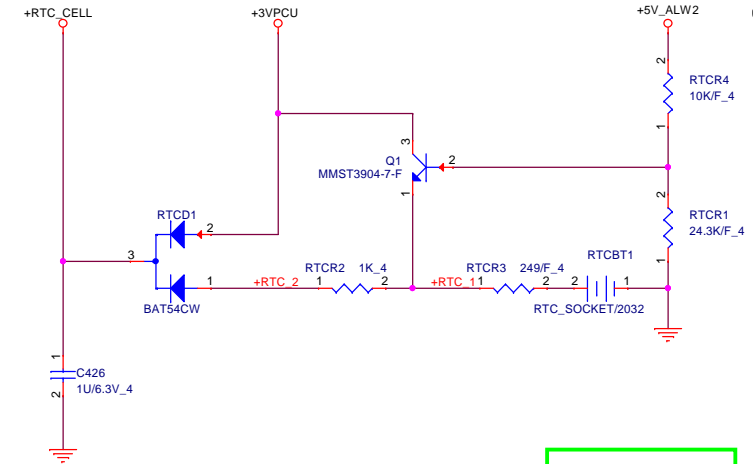
## For Skylake 8M+4M Byte

### For EC 64Mbit (8M Byte)



## RTC BATTERY

34

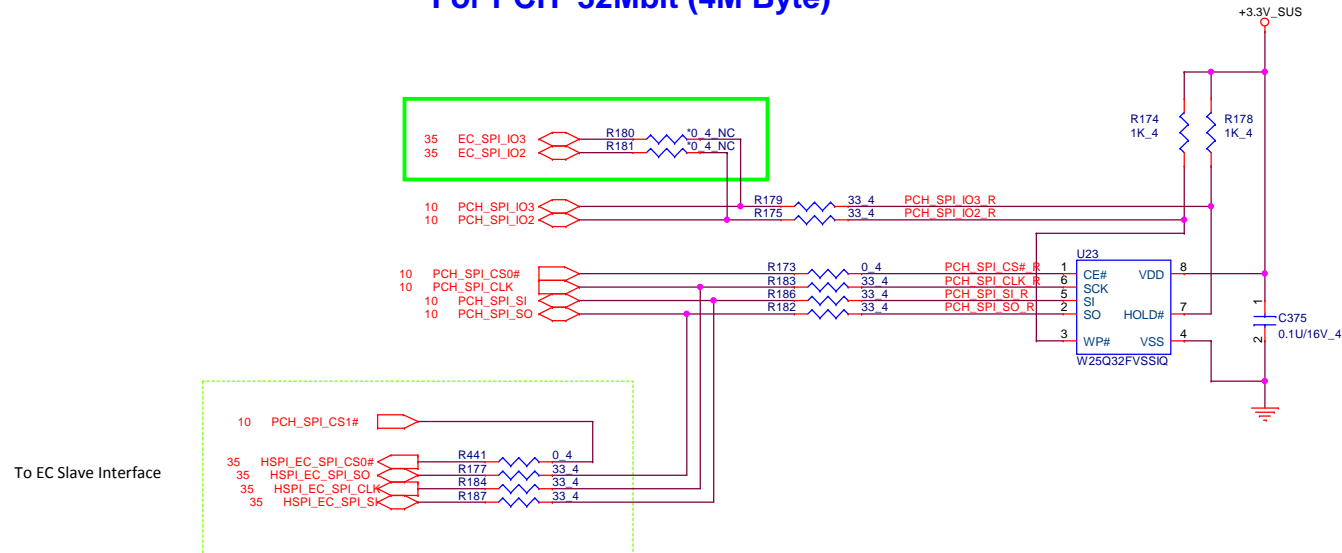


$$5 * [24.3 / (24.3 + 10)] - 0.8 = 2.74V$$

RTC Battery Charger when lower than 2.74V

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### For PCH 32Mbit (4M Byte)



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# 3VALW ON POWER LOGIC(FSW)

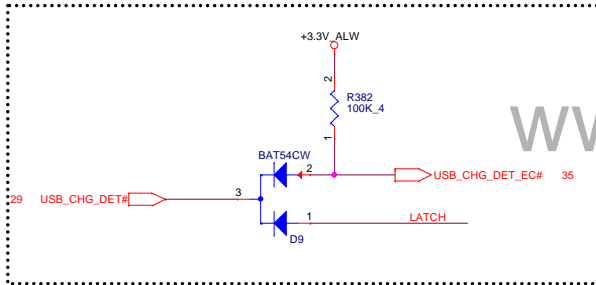
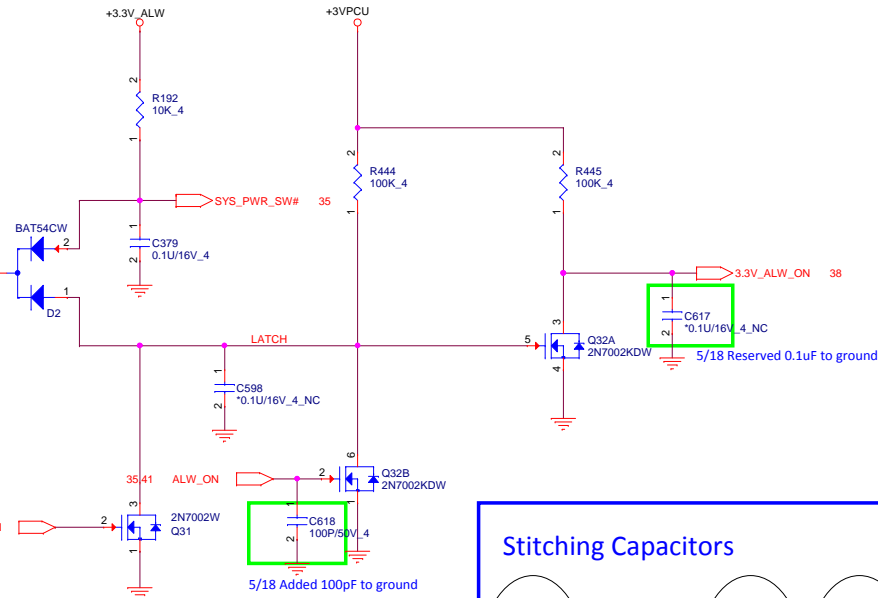
36

## POWER BUTTON

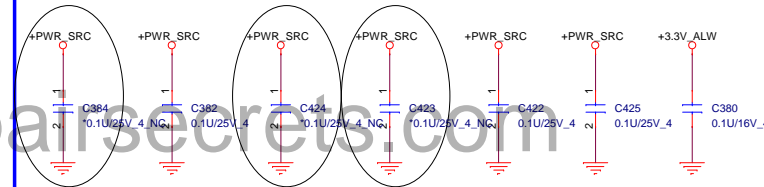
from IO board

32 POWER\_SW\_IN0#

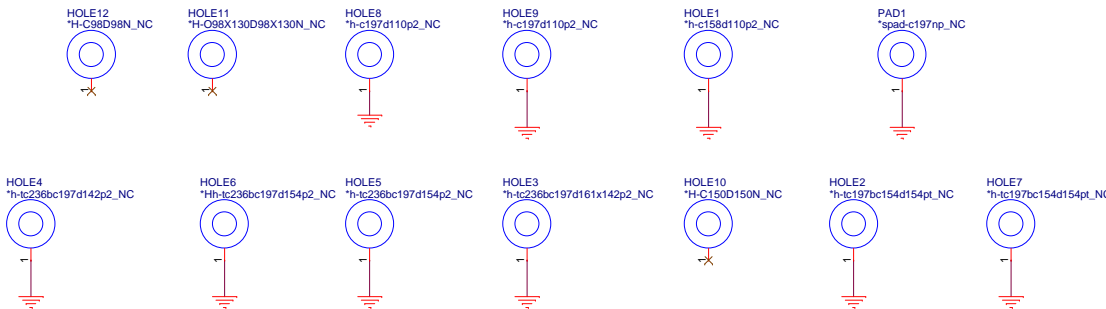
POWER\_SW\_IN0#



## Stitching Capacitors



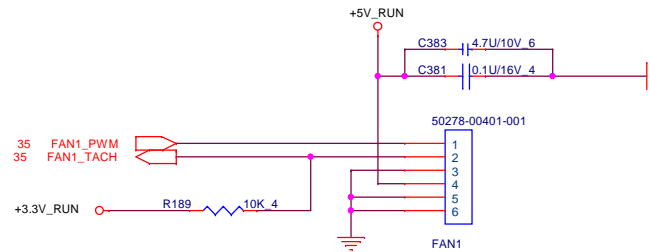
## HOLE(OTH)



stand off

HOLE13  
H-TC189BC142D142P2

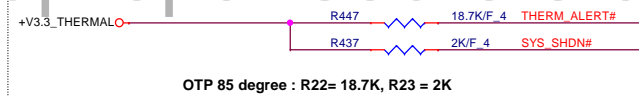
+5V\_RUN  
Max Current : 500mA  
0213 FAN connector used DFHD04MR237



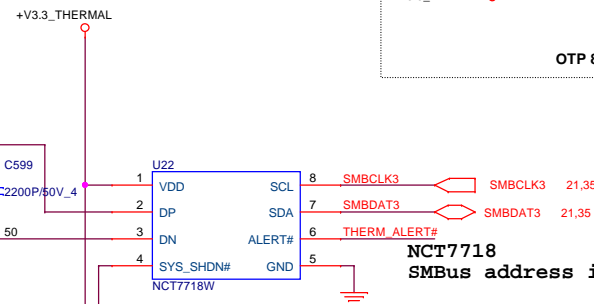
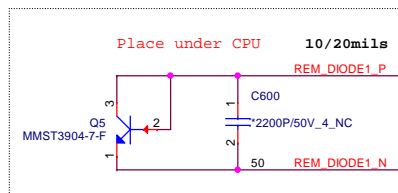
## THERMAL IC (THM)

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OTP 85 degree C



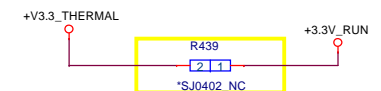
Need closed to CPU



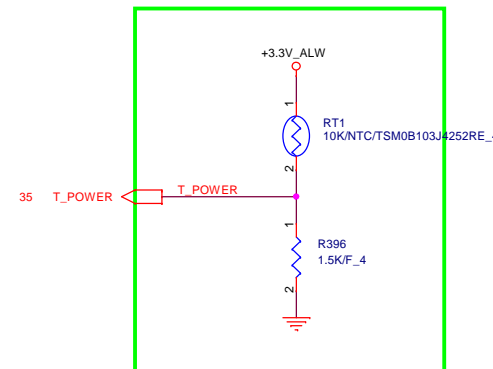
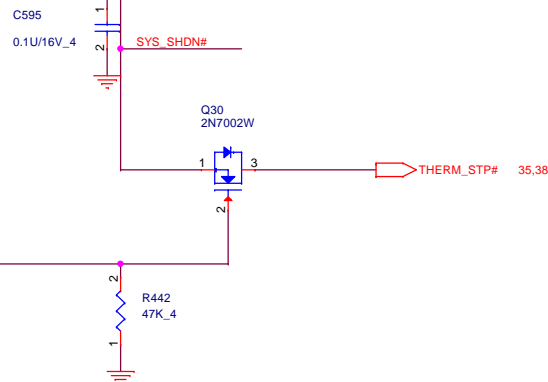
NCT7718  
SMBus address is 1001100xb (98h) (x is R/W bit).

SYS_SHDN#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

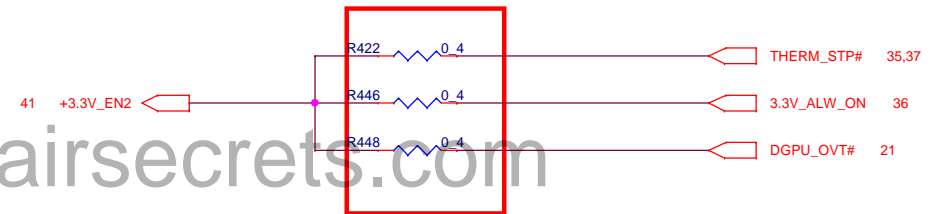
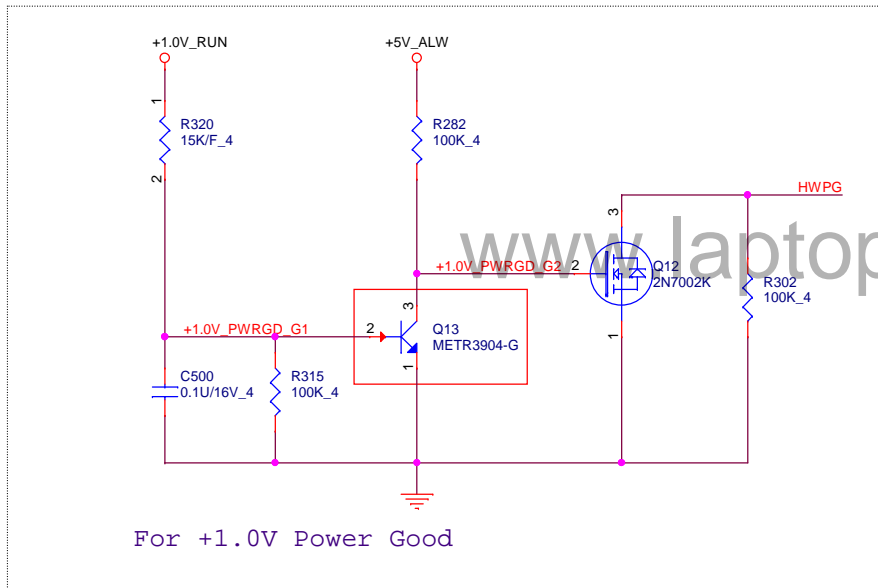
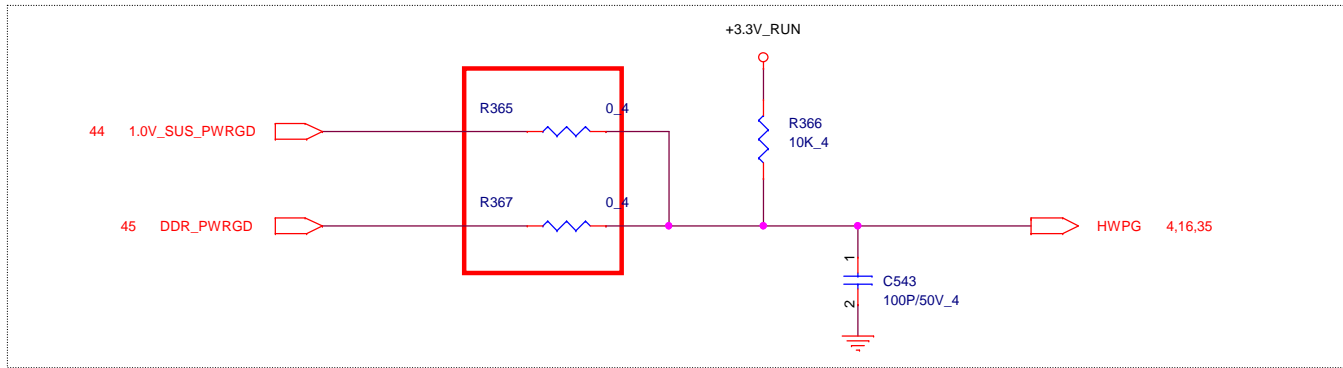
+V3.3\_THERMAL  
Max Current :mA



4,35 EC\_PWROK



## System Reset Circuit



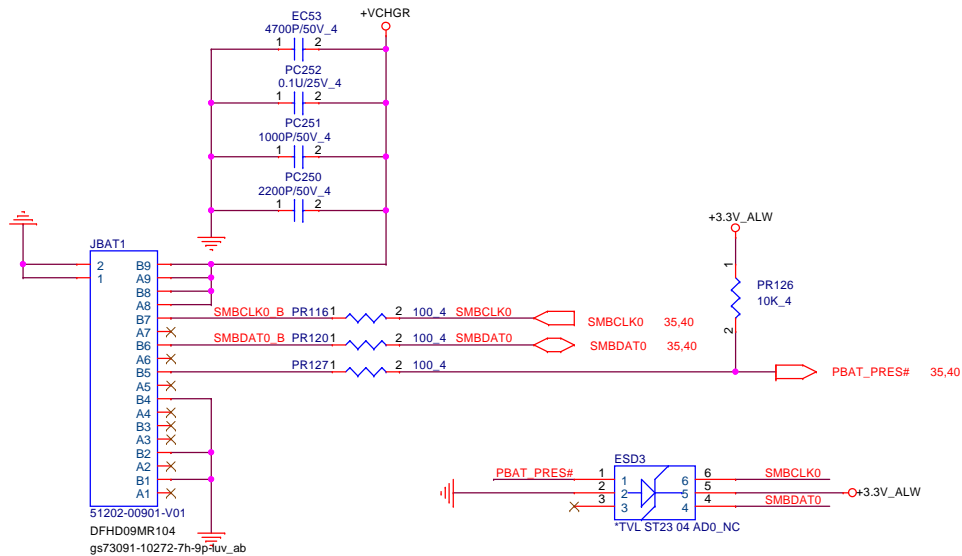
**Quanta Computer Inc.**

**PROJECT : AM8**

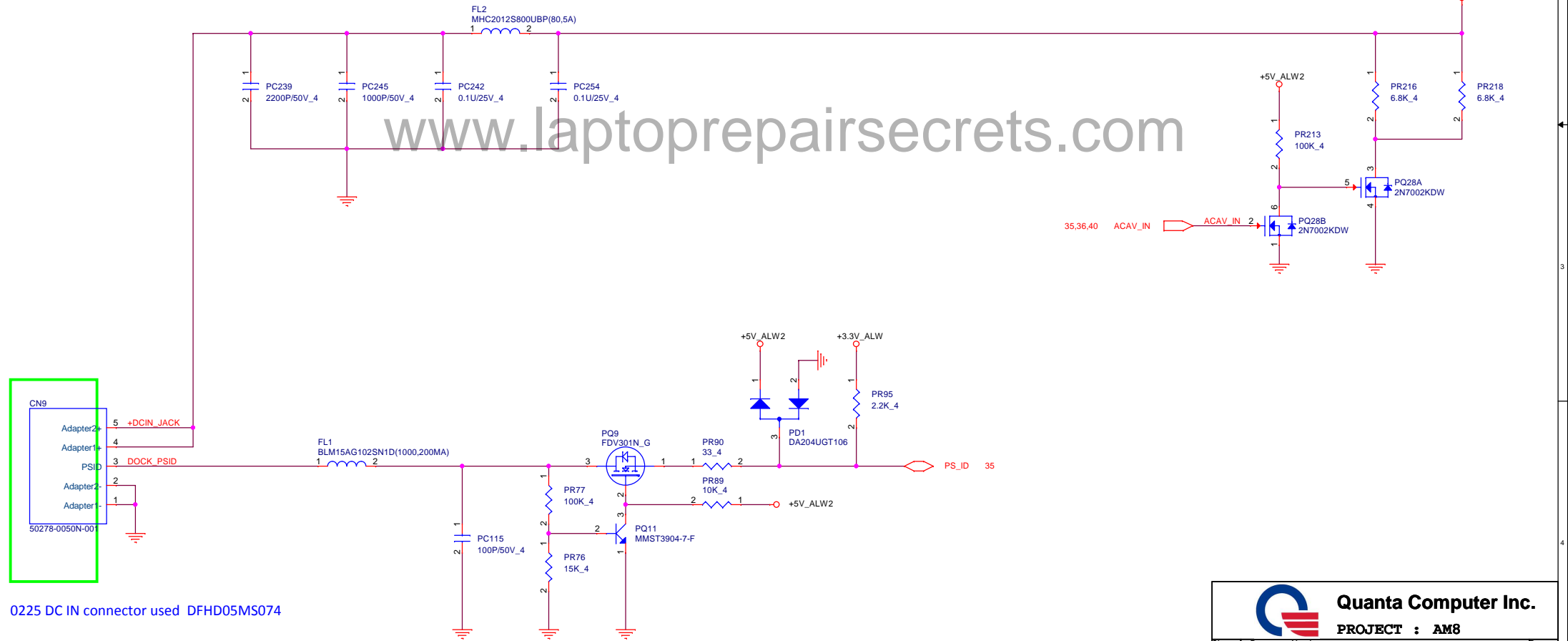
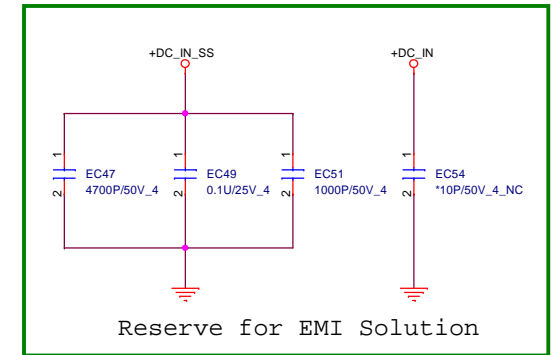
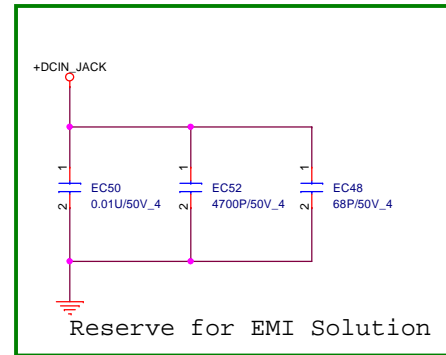
**System Reset Circuit**

Size	Document Number	Rev 1A
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0213 Battery connector used DFHD09MR104

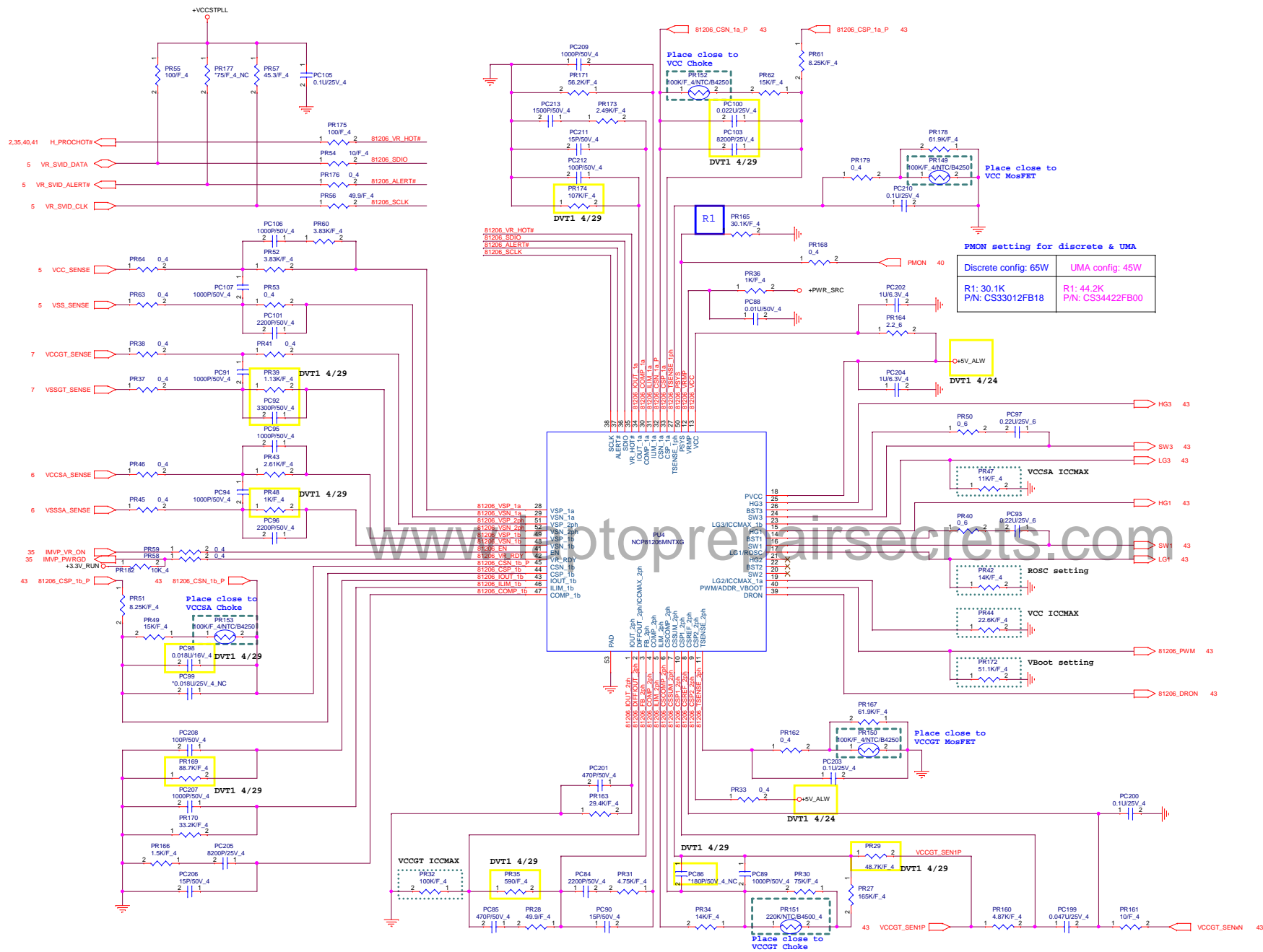


0225 DC IN connector used DFHD05MS074

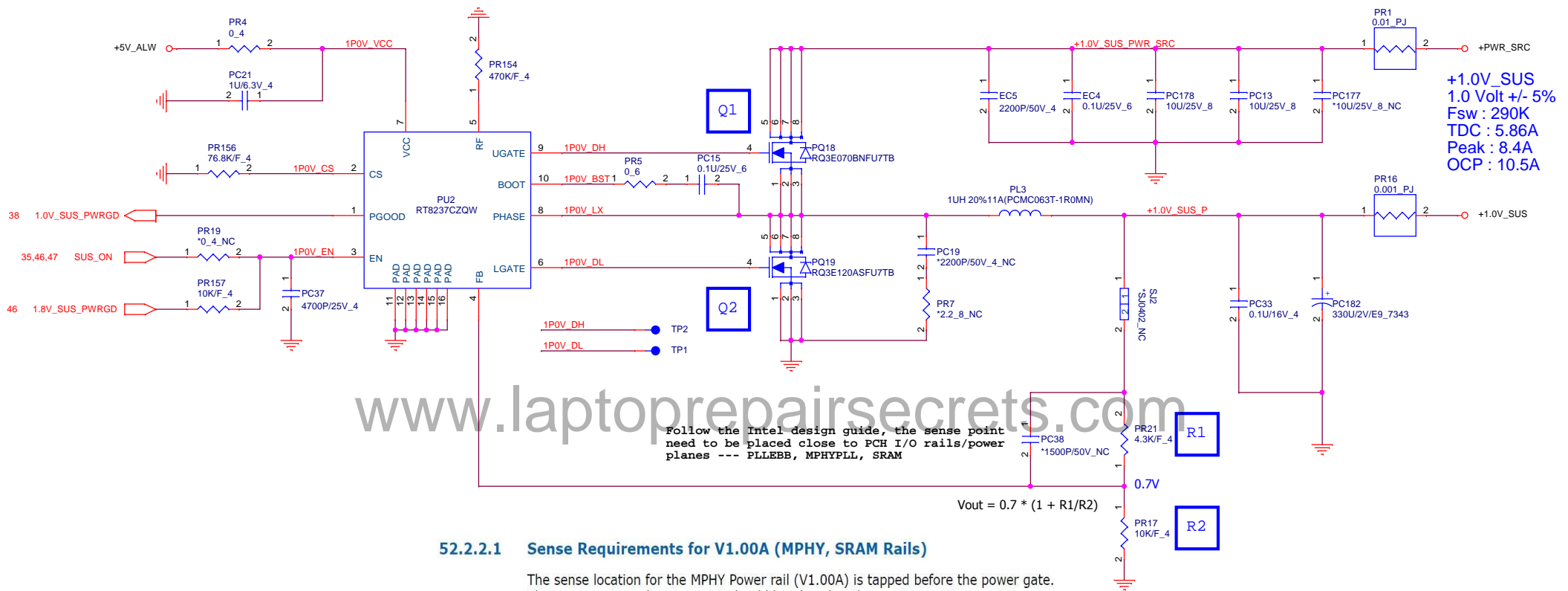












### 52.2.2.1 Sense Requirements for V1.00A (MPHY, SRAM Rails)

The sense location for the MPHY Power rail (V1.00A) is tapped before the power gate. The power gate and sense point should be placed at the maximum 13 mm - 17 mm away from the MPHY and SRAM pins. The width of this shape should be at least 15mils. This is required to meet the Vmin at the bumps.



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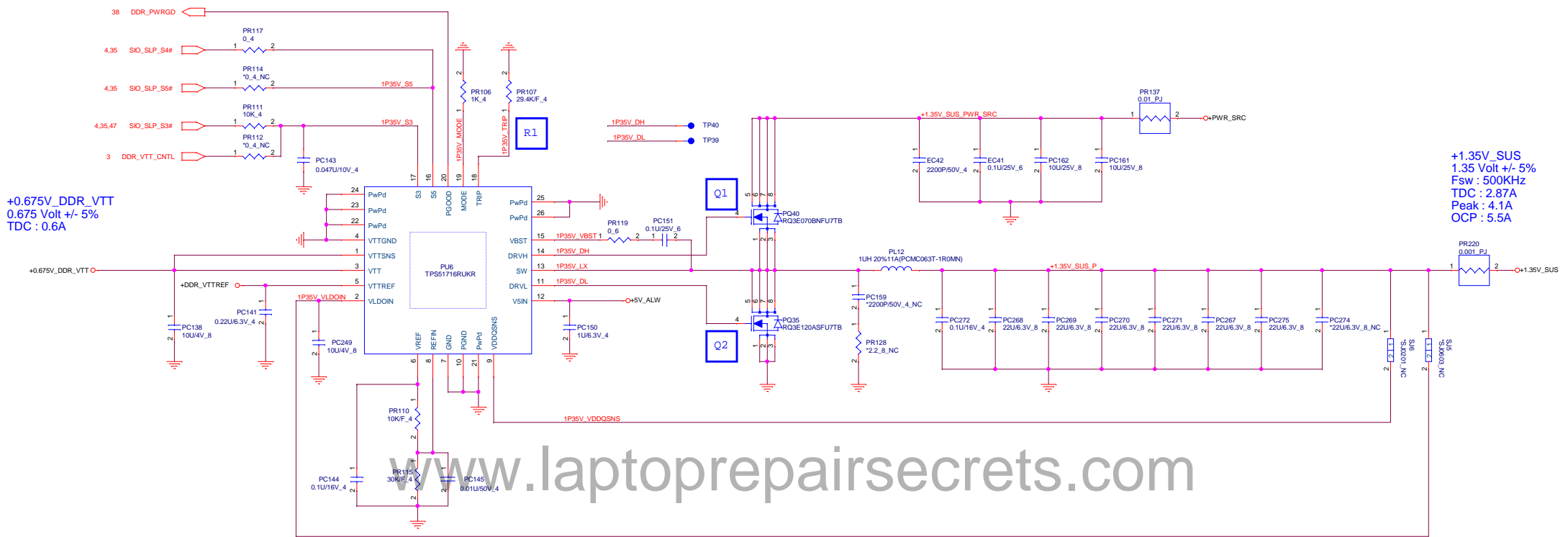
**PROJECT : AM8**

Size	Document Number	Rev
	<b>+1.0V_SUS (RT8237CZQW)</b>	1A


Date: Friday, May 22, 2015 Sheet 44 of 53

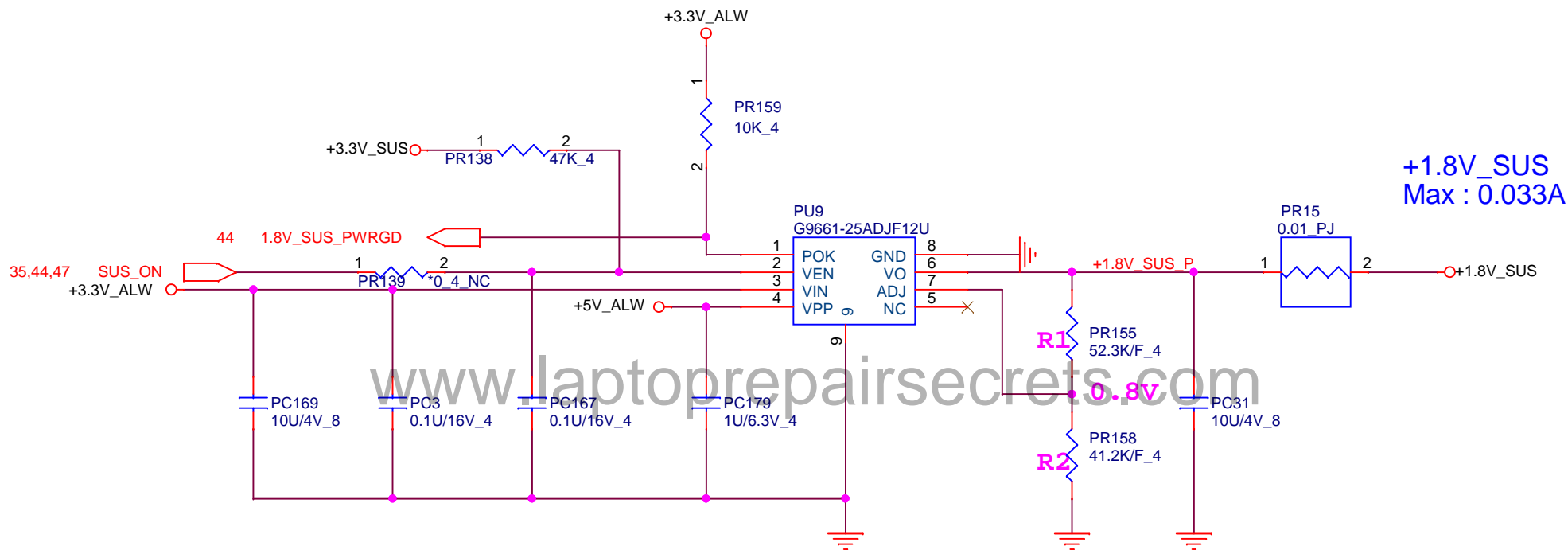
+0.675V\_DDR\_VTT  
0.675 Volt +/- 5%  
TDC : 0.6A

+1.35V\_SUS  
1.35 Volt +/- 5%  
Fsw : 500KHz  
TDC : 2.87A  
Peak : 4.1A  
OCP : 5.5A



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 <b>Quanta Computer Inc.</b> <b>PROJECT : AM8</b>		Size	Document Number	Rev	
			<b>1.35V_SUS/0.675V(TPS51716RUKR)</b>	1A	
Date:	Friday, May 22, 2016	Sheet	45	of	53



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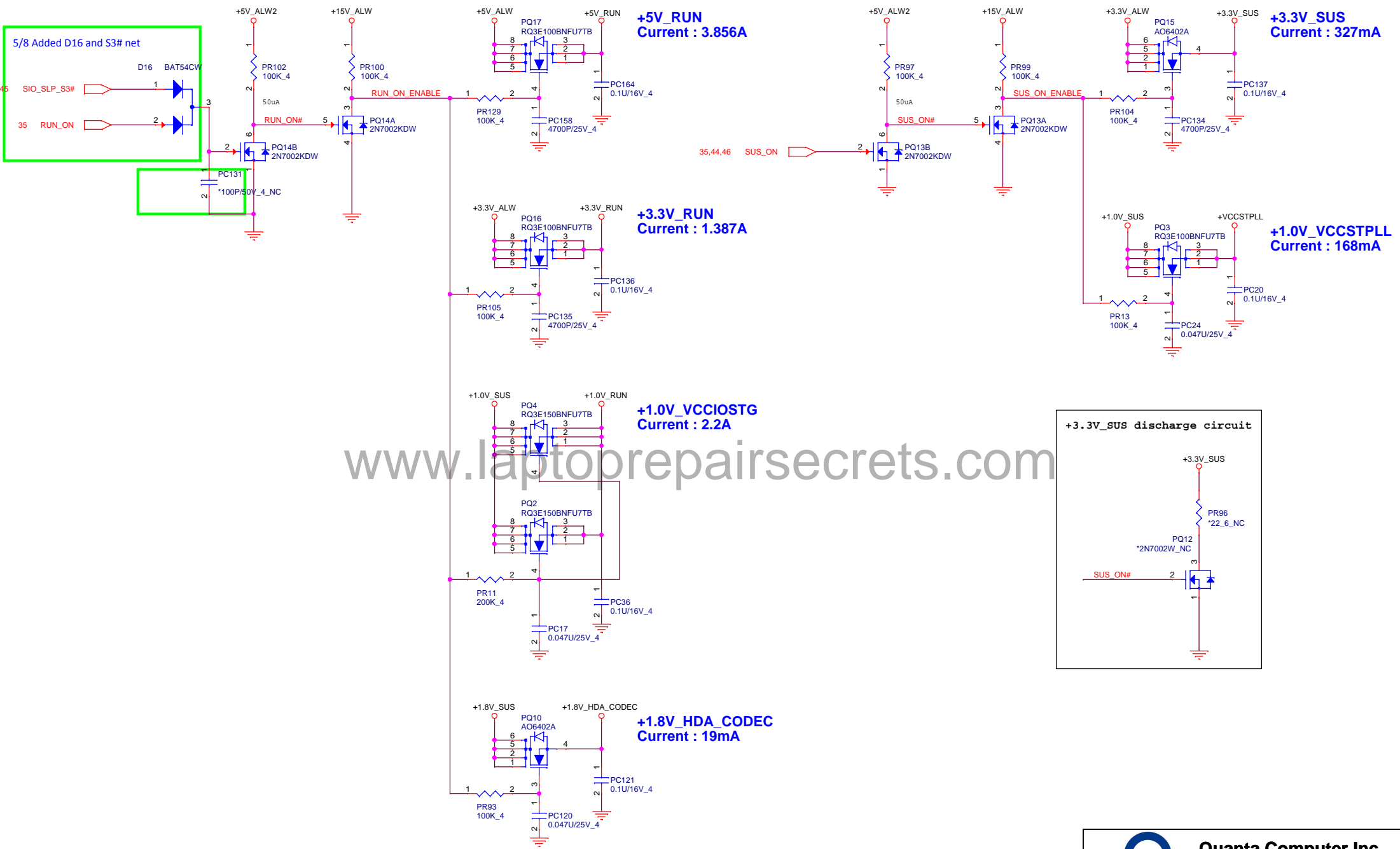
**PROJECT : AM8**

Size	Document Number	Rev
	<b>+1.8V_SUS (G9661-25ADJF12U)</b>	1A
Date:	Friday, May 22, 2015	Sheet 46 of 53

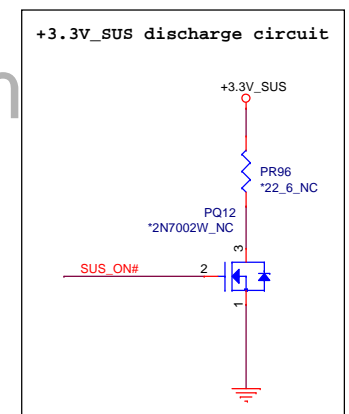
5/8 Added D16 and S3# net

SIO\_SLP\_S3#

35 RUN\_ON

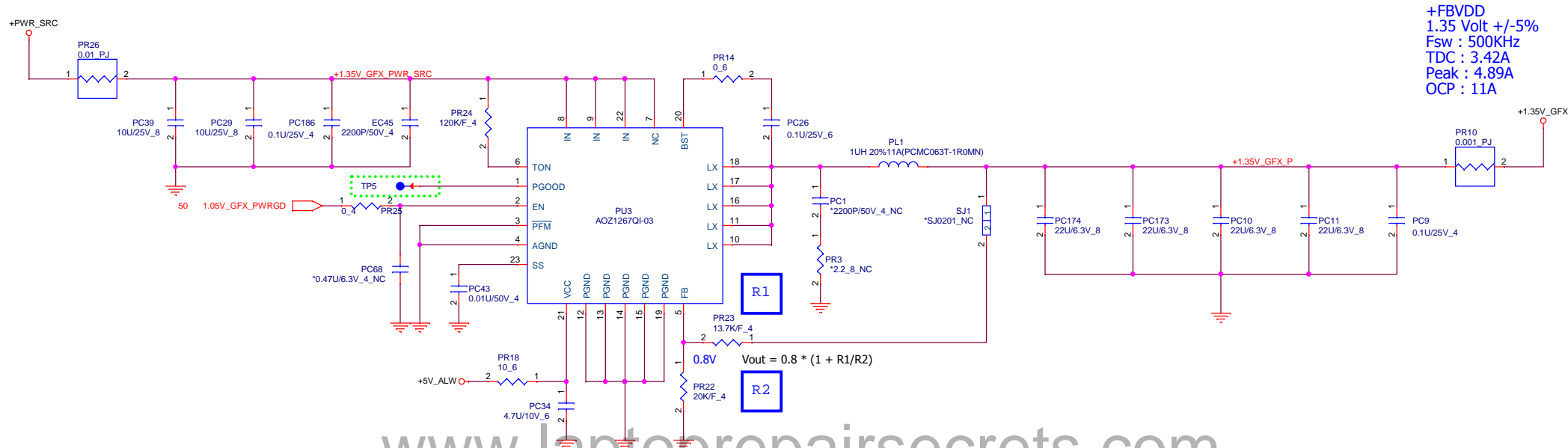


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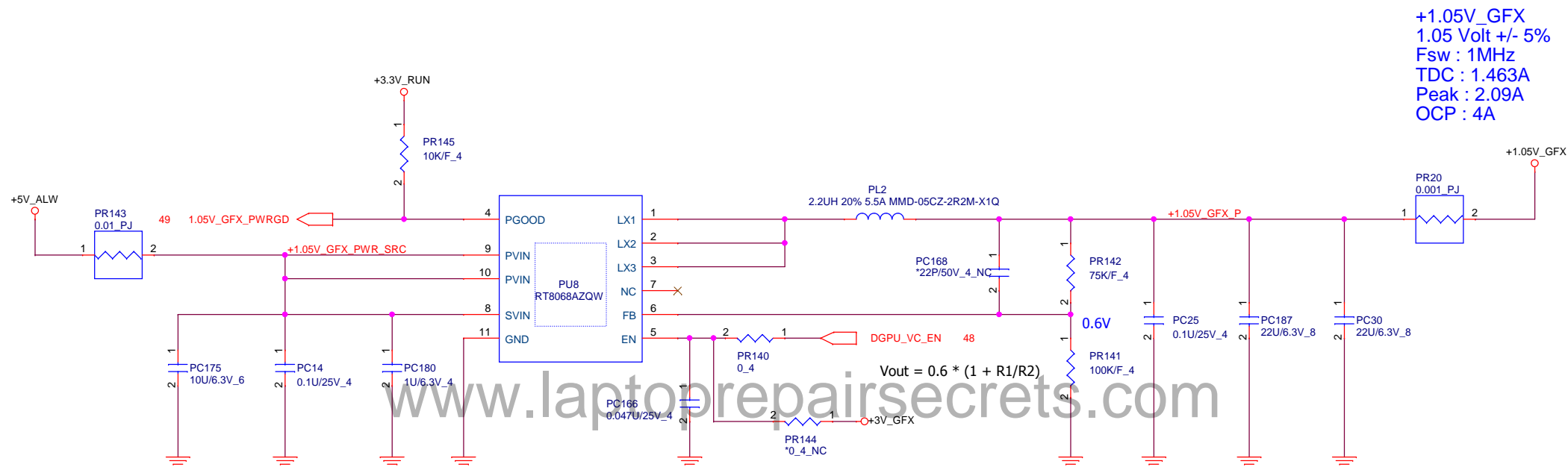


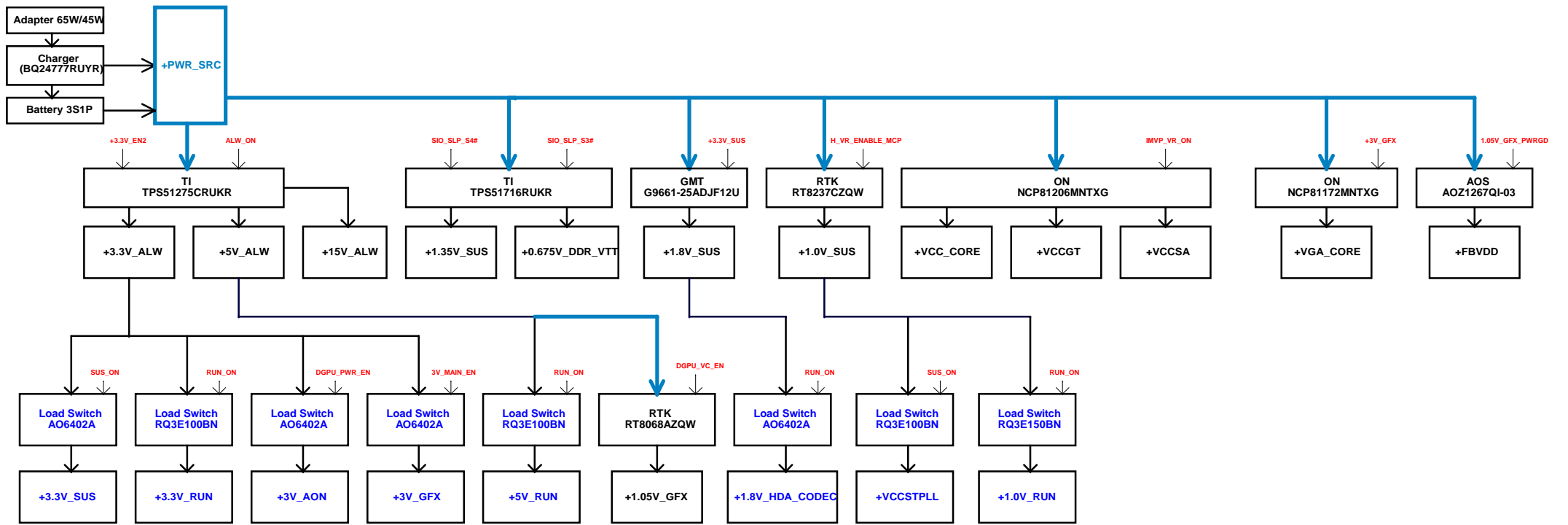




+FBVDD  
1.35 Volt +/-5%  
Fsw : 500KHz  
TDC : 3.42A  
Peak : 4.89A  
OCP : 11A

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## +PWR\_SRC



# AM9 PSequence G3 to S0 Block (Battery mode)

